VESA®

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VESA Advanced Feature Connector (VAFC) Standard

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Purpose

To standardize an open hardware interface for a high bandwidth (150 MB/sec) point-to-point connection system for transferring pixel data between graphics and video systems. The interface features limited compatibility with the current VESA Standard VGA Passthrough Connector. This document describes the architecture, timing, electrical, physical specification, and baseline operation that allows users to interchange VAFC based products from different manufacturers.

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Support for this Specification

If you have a product which incorporates VAFC, you should ask the company that manufactured your product for assistance. If you are a display or controller manufacturer, VESA can assist you with any clarification you may require. All questions must be in writing to VESA, in order of preference:

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VAFC Workgroup Members

Any industry standard requires input from many sources. The people listed below were members of the VAFC Work group of the VESA Advanced Media Interface Committee which was responsible for combining all the industry input into this standard:

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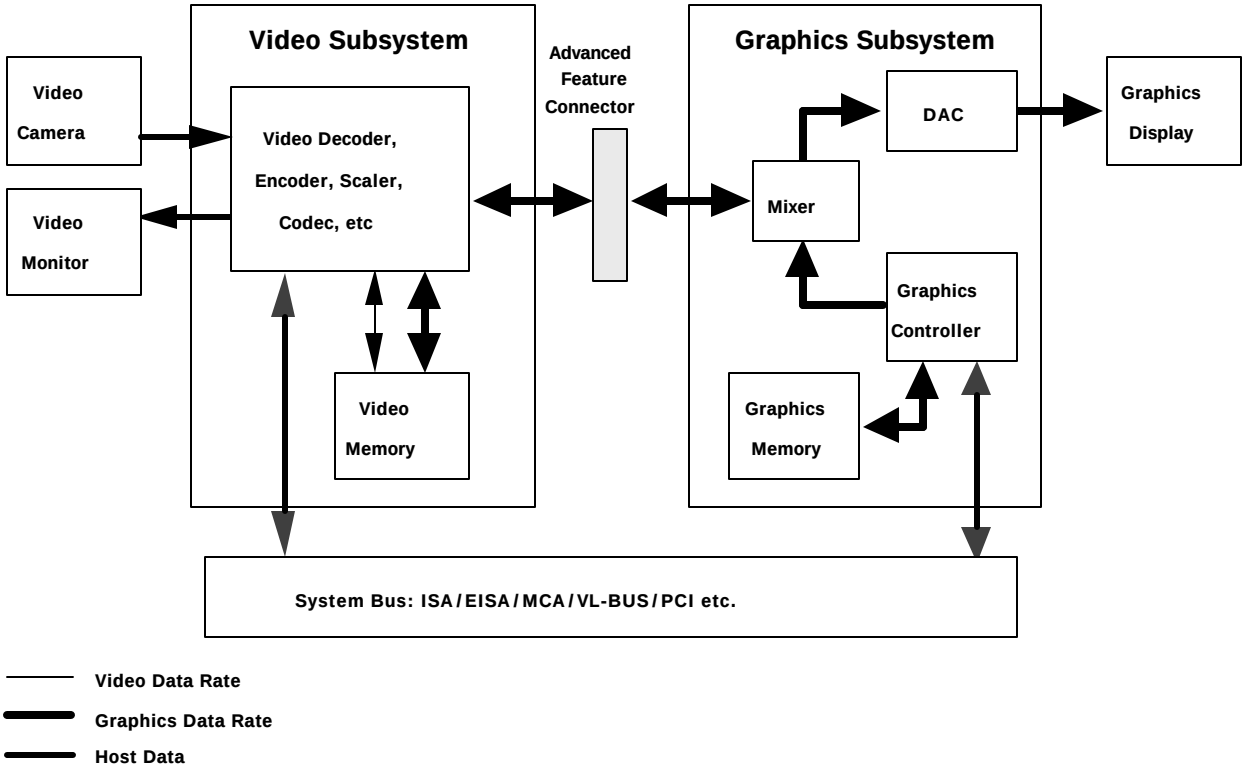
1.0 Introduction and Scope

Video is quickly making inroads into the PC and is becoming a standard data type in major operating systems. Video capture, overlay, compression and playback can now be dealt with through a standardized software interface without concern for the underlying hardware. This is a significant enhancement to the PC, and insures rapid growth in applications.

Many new hardware and software products are starting to appear featuring video capture, overlay, compression, decompression, genlock, etc. Unfortunately, each product has a proprietary hardware and software interface, limiting market growth. A particularly severe problem is that most video overlay products require the graphics system to be in a standard VGA mode, while the market has clearly embraced accelerators that support higher resolutions and color depths.

Since it is probable that a user will purchase video and graphics hardware from different vendors, there is a need to fully decouple the video and graphics systems through independent drivers. In addition, the current 8-bit VESA Standard VGA Passthrough Connector (VSVPC) is not useful beyond 256 colors at 640x480 pixel screen resolution. A new feature connector is proposed, which allows high bandwidth data exchange between the video and graphics systems, while allowing the two systems to be designed and built independently. This new connector allows transfer of video pixel data, either synchronously (in baseline configuration) or asynchronously (through extended modes) between a graphics and video subsystem with a throughput of up to 150 megabytes/second.



Typical VAFC Applications

2.0 Design Features

- Open system - Allows independently developed graphics and video systems.
- Robust set of signals available for both baseline and high-end applications.
- Bi-directional (one direction per transfer, no split-direction transfers allowed) 32/16-bit wide data bus, 37.5 MHz maximum clock rate, 150 Mbyte/s maximum bandwidth.
- Supports video overlay up to 1024x768 graphics with baseline 16-bit bus.
- Low additional cost to graphics system .
- Supports video overlay on graphics, graphics output to video, with the possibility of genlocking to an external video source.
- Supports limited backward output-only compatibility with the 8-bit VESA Standard VGA Passthrough Connector (VSVPC).
- Features a well-defined baseline for guaranteed minimal compatibility, extended modes available through software configuration.
- All pixel data travels with its own clock to eliminate clock skew.
- Two devices supported up to 7" apart - one graphics, one video.
- All video functionality, such as compression or multiple stream support, is implemented on the video system.
- Uses industry standard connectors and ribbon cable.

3.0 Pin Description Table

Name: Where a signal is identical to the VESA Standard VGA Passthrough Connector (VSVPC) signal in 8-bit mode, that name is used in this standard to emphasize compatibility.

Direction Control: Shows which pin, if any, controls the I/O direction of the pin

Video Mode:

"**In**" means data is coming **into** the graphics system from the video system.
"**Out**" means data is going **out** of the graphics system into the video system.

I/O: Table entry refers to the electrical pin functionality in a particular mode. Pin directions are defined as seen at the graphics system . For any table entry, the video system I/O direction is opposite that shown for the graphics system .

Sync: Table entry indicates if the pin is synchronous to DCLK or VCLK or neither.

Name	Direction Control	Video Mode	I/O	Sync	Description
P31:0 data	EVIDEO*	In	I	VCLK	Data from video system , P31:0 or P15:0
		Out	O	DCLK	Data from graphics system, P31:0, P15:0 or P7:0
DCLK graphics clock	-	In/Out	O	-	Continuous master clock driven from the graphics system to the video system , typically based on DAC pixel clock, or a sub multiple thereof. Used as reference for graphics data.
VCLK video clock	-	In/Out	I	-	Continuous master clock driven from the video system to the graphics system . Used as reference for video data and related handshake lines.
BLANK* blank	-	In/Out	O	DCLK	Low indicates the graphics system is in the blanked region.
HSYNC horizontal sync	-	In/Out	O	DCLK	Graphics horizontal sync sent to video system as basic display framing reference signal
VSYNC vertical sync	-	In/Out	O	DCLK	Graphics vertical sync sent to video system as basic display framing reference signal.
EVIDEO* enable external video data	-	In	I	-	Driven active low by video system to drive P31:0 into graphics system
		Out	I	-	Pulled passive high by graphics system to drive P31:0 into video system
EGEN* enable genlock	-	In/Out	I	-	Pulled low by video system to enable genlock clock input on GENCLK.
GRDY graphics ready	-	In	O	VCLK	Indicates graphics system is ready to latch the data on the bus.
VRDY video ready	-	In	I	VCLK	Indicates video system has placed valid data on the bus.
FSTAT FIFO status	-	In	O	VCLK	Indicates FIFO has reached a predetermined level
OFFSET 1:0 pixel offset	-	In	I	VCLK	Allows single pixel alignment in multipixel formats

GENCLK Genlock input	-	In/Out	I	-	Genlock input clock to graphics controller
RSRV2:0	TBD	TBD	TBD	TBD	Reserved for future definition
GND	-	-	-	-	Connect to ground plane on both cards
Total: 80					

4.0 Signal Descriptions

4.1 P31:0

These are the data lines. In 16-bit mode only P15:0 are used. In VSVPC 8-bit passthrough compatibility mode only P7:0 are used, and they map directly to P7:0 of the VSVPC.

Lines which are unused in a particular mode may be floated by the source, but the sense of EVIDEO* must be observed if the lines are driven. Any data may appear on unused lines and should be ignored by the destination.

The data formats and pixel to connector pin assignments for both baseline and extended modes are listed in the following tables:

4.1.1 8-Bit Transfer Modes

4.1.1.1 8-Bit Indexed, one pixel per clock (Baseline output mode)

P	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Data	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

P	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data	X	X	X	X	X	X	X	X	P07	P06	P05	P04	P03	P02	P01	P00

4.1.2 16-Bit Transfer Modes

4.1.2.1 8-Bit Indexed, two pixels per clock (Extended mode)

P	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Data	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

P	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00

4.1.2.2 15-Bit RGB, 5:5:5, one pixel per clock (Extended mode)

P	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Data	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

P	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Data	X	P0 R4	P0 R3	P0 R2	P0 R1	P0 R0	P0 G4	P0 G3	P0 G2	P0 G1	P0 G0	P0 B4	P0 B3	P0 B2	P0 B1	P0 B0

4.1.2.3 16-Bit RGB, 5:6:5, one pixel per clock (Baseline Input Mode)

P	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Data	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

P	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data	P0 R4	P0 R3	P0 R2	P0 R1	P0 R0	P0 G5	P0 G4	P0 G3	P0 G2	P0 G1	P0 G0	P0 B4	P0 B3	P0 B2	P0 B1	P0 B0

4.1.3 32-Bit Transfer Modes

4.1.3.1 8-Bit Indexed, four pixels per clock (Extended mode)

P	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Data	P3 7	P3 6	P3 5	P3 4	P3 3	P3 2	P3 1	P3 0	P2 7	P2 6	P2 5	P2 4	P2 3	P2 2	P2 1	P2 0

P	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data	P1 7	P1 6	P1 5	P1 4	P1 3	P1 2	P1 1	P1 0	P0 7	P0 6	P0 5	P0 4	P0 3	P0 2	P0 1	P0 0

4.1.3.2 15-Bit RGB, 5:5:5, two pixels per clock (Extended mode)

P	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Data	X	P1 R4	P1 R3	P1 R2	P1 R1	P1 R0	P1 G4	P1 G3	P1 G2	P1 G1	P1 G0	P1 B4	P1 B3	P1 B2	P1 B1	P1 B0

P	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data	X	P0 R4	P0 R3	P0 R2	P0 R1	P0 R0	P0 G4	P0 G3	P0 G2	P0 G1	P0 G0	P0 B4	P0 B3	P0 B2	P0 B1	P0 B0

4.1.3.3 16-Bit RGB, 5:6:5, two pixels per clock (Extended mode)

P	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data	P1 R4	P1 R3	P1 R2	P1 R1	P1 R0	P1 G5	P1 G4	P1 G3	P1 G2	P1 G1	P1 G0	P1 B4	P1 B3	P1 B2	P1 B1	P1 B0

P	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data	P0 R4	P0 R3	P0 R2	P0 R1	P0 R0	P0 G5	P0 G4	P0 G3	P0 G2	P0 G1	P0 G0	P0 B4	P0 B3	P0 B2	P0 B1	P0 B0

4.1.3.4 24-Bit RGB, 8:8:8, one pixel per clock (Extended mode)

P	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data	X	X	X	X	X	X	X	X	P0 R7	P0 R6	P0 R5	P0 R4	P0 R3	P0 R2	P0 R1	P0 R0

P	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data	P0 G7	P0 G6	P0 G5	P0 G4	P0 G3	P0 G2	P0 G1	P0 G0	P0 B7	P0 B6	P0 B5	P0 B4	P0 B3	P0 B2	P0 B1	P0 B0

4.1.3.5 32-Bit RGB+Alpha, 8:8:8:8, one pixel per clock (Extended mode)

P	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data	P0 A7	P0 A6	P0 A5	P0 A4	P0 A3	P0 A2	P0 A1	P0 A0	P0 R7	P0 R6	P0 R5	P0 R4	P0 R3	P0 R2	P0 R1	P0 R0

P	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data	P0 G7	P0 G6	P0 G5	P0 G4	P0 G3	P0 G2	P0 G1	P0 G0	P0 B7	P0 B6	P0 B5	P0 B4	P0 B3	P0 B2	P0 B1	P0 B0

4.1.4 YCrCb Pixel Modes

4.1.4.1 Component Ordering

All YCrCb data format are extended modes.

The YCrCb formats should be encoded as per CCIR Recommendation 601 levels. In 16-bit YCrCb 4:2:2 pixel modes two pixel clocks are required to transfer both luminance and chrominance data for two pixels.

In synchronous designs, where there is a one-to-one correspondence between DCLK and VCLK, the zero'th YCrCb clock is defined as the first video pixel data transferred after the trailing edge of HSYNC on each scan line. In asynchronous designs, where there is no fixed relationship between DCLK and VCLK, the zero'th YCrCb clock is defined as the first video pixel transferred after the trailing edge of VSYNC. YCrCb data must be delivered in a continuous component order stream, with no interruption of the CbYCrYCb... order from scan line to scan line. The data for each scan line must begin with a CbY pair and end with a CrY pair to insure that the stream stays in synchronization. Color space interpolators must reset at the end of each scan line to avoid corrupting the first pixel of the following scan line.

In 16-bit YCrCb 4:2:2 pixel modes, two pixels are transferred every two clocks with component order:

Clock #	**0**	**1**	**2**	**3**	**4**	**5**	**6**	
P7:0	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4	Cb6	etc.
P15:8	Y0	Y1	Y2	Y3	Y4	Y5	Y6	

In 24-bit YCrCb 4:4:4 pixel modes, one pixel is transferred per clock with component order:

Clock #	**0**	**1**	**2**	**3**	**4**	**5**	**6**	
P7:0	Cb0	Cb1	Cb2	Cb3	Cb4	Cb5	Cb6	
P15:8	Y0	Y1	Y2	Y3	Y4	Y5	Y6	etc.
P23:16	Cr0	Cr1	Cr2	Cr3	Cr4	Cr5	Cr6	
P31:24	-	-	-	-	-	-	-	

In 32-bit YCrCb 4:2:2 pixel mode, two pixels are transferred per clock with component order:

Clock #	**0**	**1**	**2**	**3**	**4**	**5**	**6**	
P7:0	Cb0	Cb2	Cb4	Cb6	Cb8	Cb10	Cb12	
P15:8	Y0	Y2	Y4	Y6	Y8	Y10	Y12	etc.
P23:16	Cr0	Cr2	Cr4	Cr6	Cr8	Cr10	Cr12	
P31:24	Y1	Y3	Y5	Y7	Y9	Y11	Y13	

4.2 EVIDEO*

EVIDEO* controls the direction of the P31:0 lines. It has a passive pull-up on the graphics system, and is pulled low with an open collector or totem-pole driver on the video system. If a open collector driver is used the video card should also passively pull up this signal.

The following table lists the functions of the direction pin:

Signal	State	Function
EVIDEO*	HIGH	Pixel data on P31:0 driven from graphics board to video board
	LOW	Pixel data on P31:0 driven from video board to graphics board

4.3 DCLK, VCLK

DCLK is the clock output from the graphics system which defines the speed of the interface, and must be limited to <= 37.5 MHz. All data output from a graphics system to a video system is referenced to the rising edge of DCLK. In most modes it is the basic DAC pixel clock, or a /2 submultiple thereof.

VCLK is the clock which is output from the video system, and must be limited to <= 37.5 MHz. All data output from a video system to a graphics system is referenced to the rising edge of VCLK.

4.4 GRDY, VRDY

GRDY is asserted high by the graphics system to indicate to the video system that the graphics system is ready to receive data.

VRDY is asserted high by the video system to indicate to the graphics system that the video system is presenting valid data on the P31:0 pins.

Data from the video system is latched by the graphics system when both GRDY and VRDY are sampled high during a rising edge of VCLK.

In extended modes, GRDY and VRDY can also be used in a cycle-by-cycle handshake mode for supporting graphics systems that include FIFOs for asynchronous video input operation.

There is no support for cycle-by-cycle FIFO handshake operations for output from a graphics to a video system.

4.5 HSYNC, VSYNC, BLANK*

BLANK* defines the display area. HSYNC may be used for line counting. VSYNC may be used as a master field-by-field reset. HSYNC and VSYNC must both be fully contained within the blanked display area.

The polarity and timing of HSYNC and VSYNC will vary unpredictably with the monitor timing and graphics video mode. Blank can be used to acertain the polarity of HSYNC and VSYNC. The following rules must be observed for correct operation:

- In baseline VSVPC-compatible output mode, timing with respect to DCLK is unspecified and may vary from one graphics system to another.
- All three signals must be delivered by the graphics system synchronous with DCLK in all modes.
- Monitor HSYNC and VSYNC may be used if they meet the Tod and Toh specifications.
- BLANK* must truly define the displayed and blanked areas.
- BLANK* must define only one contiguous rectangle per vertical sync.
- The blanked region must fully enclose the vertical and horizontal sync.
- The video system should use the first edge of HSYNC which occurs after BLANK* goes low on each line to determine the start of the HSYNC period.
- If an HSYNC edge occurs in the same cycle where BLANK* falls, use that edge.
- The video system should use the first edge of VSYNC which occurs after BLANK* goes low to determine the start of the VSYNC period.
- If a VSYNC edge occurs in the same cycle where BLANK* falls, use that edge.

Interlaced graphics modes are **not** supported in the VESA VAFC definition.

GRDY, VRDY and BLANK* ***must not*** make any extraneous transitions, i.e. they should be output from synchronous rather than combinatorial logic. This is very important as video systems may use these signals to gate DCLK (in some way) when driving VRAM serial clocks.

HSYNC and VSYNC should not have spurious edges as these will disturb the monitor.

4.6 OFFSET1:0 Pixel Offset

OFFSET1:0 may be output by a video system in an extended mode where both DCLK is 1/2 of the graphics pixel clock, and two pixels are being delivered per clock. Normally this would force a 4-pixel granularity of the video overlay. Using the OFFSET1:0 pins, the video board can specify that the video data should be shifted right from zero to three pixels, thus allowing positioning of the video window on an arbitrary pixel boundary.

The value of OFFSET1:0 may change on a per VCLK basis but in general will be a constant value for each video window and will only change on a per video window basis. OFFSET1:0 must be clocked with the pixel data that it is affecting.

The mapping of OFFSET1:0 to the pixel shift value is listed in the following table:

OFFSET1	OFFSET0	Pixel Shift
1	1	0
1	0	1
0	1	2
0	0	3

4.7 FSTAT

FSTAT may be used by a graphics board that has a video pixel FIFO to indicate that the FIFO fullness has reached a predefined level. Both the FIFO size and watermark level must be determined or negotiated via the configuration software. A graphics system that does not implement this feature should drive this pin low or wire it to ground.

4.8 GENCLK

GENCLK is a dotclock input to the graphics system for genlock (NTSC, PAL, and SECAM video synchronization) applications. In general, this input will be fed either into the external frequency input of the dotclock chip on the graphics system, or if the graphics controller incorporates a dotclock frequency synthesizer, directly into the external frequency input of the controller. The video system adjusts the frequency of the GENCLK signal so that the graphics system is genlocked to a composite signal (NTSC, PAL, or SECAM) received by the graphics system. Genlock occurs when the HSYNC and VSYNC from the graphics system (rate of which is controlled by GENCLK rate) aligns to the HSYNC and VSYNC detected in the composite signal. It is the responsibility of the video system to perform composite signal sync seperation, video and graphics sync comparison, and GENCLK synthesis.

Genlocking allows overlay and mixing of graphics and video without the requirement of a separate frame buffer. To be compatible with composite video signal (lines per frame), the graphics system should display a total of 525 non-interlaced vertical lines for NTSC type output and a total of 625 non-interlaced vertical lines for PAL and SECAM type output. In genlock, the VSYNC rate will be the same as video frame rate, and the HSYNC rate will be twice the video line rate. It is the responsibility of the video system to translate the non-interlaced data from the graphics system into interlaced data (a line store is required).

A system that intends to use genlock should deliver a clock of a nominal frequency, such as 25.175 MHz, upon power up for start-up purposes. The clock may then be enabled using the EGEN* pin described below. The actual genlock frequency is not defined as a fixed value.

GENCLK is only available in extended modes and is not a baseline graphics system requirement.

4.9 EGEN*

EGEN* enables genlock clock input to the graphics controller on the GENCLK pin. It has a passive pull-up on the graphics system, and is pulled low with an open collector or totem-pole driver on the video system.

4.10 RSRV2:0

RSRV2:0 are reserved for definition by VESA to allow for future expansion. All currently defined VAFC modes function without these pins connected.

To insure compatibility with future revisions of the standard, the following rules must be followed:

- Do not connect RSRV2:0 to either power plane.
- Do not pull down RSRV2:0 with resistors. Pull-ups are allowed.
- RSRV2:0 must not be driven at power-up.

4.11 Pull-ups

Pull-up resistors between 10K and 50K ohms are required on some pins to stop signals from floating when one board is disconnected, or two boards of differing capabilities are connected. Pull-ups are allocated on each board as follows:

- If a signal is only an output it does not need a pull-up, even if the output can be disabled.
- If a signal can be an input in any mode, it must have a pull-up.
- If a signal is a no connect, such as P31:16 on a 16-bit only board, it does not need a pull-up.

Note that in some cases a signal may have two pull-ups, one on each board.

5.0 Power-Up Conditions

5.1 Graphics System Power Up Condition

A graphics system must power up as a standard VGA system with the following pins functional in output mode only: P7:0, DCLK, BLANK*, HSYNC and VSYNC. The direction of P7:0 data is controlled by EVIDEO*. Genlock is disabled. Data format is 8-bit palettized. If the graphics system changes modes to other than 8-bit palletized at less then 37.5 MHz, the output data is undefined.

5.2 Video System Power Up Condition

A VAFC video system, upon power up, may monitor the following pins if it is designed to receive 8-bit palettized data: P7:0, DCLK, BLANK*, HSYNC, and VSYNC. It must not drive any pins on the VAFC bus until enabled by a VAFC software driver.

This document does not claim to cover the standard VESA Standard VGA Passthrough Connector (VSVPC) operation. Please refer to the references in Appendix B for more information.

6.0 Baseline Operation and Requirements

A baseline graphics system **MUST** support both baseline input and output modes to be VAFC compliant.

Baseline VAFC mode has the following pins functional: P15:0, DCLK, VCLK, BLANK*, GRDY, HSYNC and VSYNC. Data direction is determined by EVIDEO*.

6.1 Baseline Output - Standard VGA Feature Connector Compatible

A VAFC graphics board must power up in baseline 8-bit palettized data output mode, which is compatible with the VSVPC with the following restrictions:

P31:8, GRDY, VRDY and OFFSET1:0 may be active, but none of these pins will connect to the VSVPC board. VRDY must be ignored in this mode.

The VSVPC 8-bit input mode is not supported.

6.2 Baseline Input

All VAFC compliant products must, at a minimum, support baseline input mode. Baseline input mode requires a 16-bit 5:6:5 RGB data format on both the graphics and video system. DCLK must be switchable under software control between 1x and 1/2x the pixel clock. The receiving graphics system will display each video pixel through 1 or 2 graphic pixel clocks as required. As an example, to overlay video on a 1024x768 display with a 75 MHz pixel clock, the video board would deliver a maximum of 512 pixels per line at 37.5 MHz, with each pixel displayed twice.

Baseline systems are required to synchronize the video data to the graphics data. As a result, the video board must use the graphics boards syncs, blanking, and clock signals. This requires that the VCLK and DCLK be of the same frequency with VCLK trailing DCLK by no less than 5ns and no more than 20 nsec.

VRDY should never be left undefined or floating. Baseline graphics boards are not required to use the VRDY signal. If a video board does not use the VRDY signal, it is required to pull it up.

Note that for N transfers, GRDY is active for N-1 transfers.

The video board must not transfer data to the graphics system if GRDY is sampled low.

After GRDY is sampled low at the end of the active line, the video board must hold the data for a minimum of one VCLK cycle. After one VCLK cycle, the video board may place the data for the first

pixel of the next line on the data bus. The data for the first pixel of the next line must be stable on the data bus upon the trailing edge of HSYNC.

The graphics system must ensure that the initial rising edge of GRDY is at least two VCLK cycles after the trailing edge of HSYNC.

6.3 Non-Baseline Pin Functionality in Baseline Mode

6.3.1 P31:16

Data is undefined in baseline modes, but direction is always controlled by EVIDEO*.

6.3.2 VRDY

A baseline-only graphics system may leave this pin as a no connect.

6.3.3 FSTAT

A baseline-only graphics system will drive this pin low or wire it to ground. A baseline/extended video system will see a low (inactive) level indicating that the FIFO has never reached the predetermined level of fullness.

6.3.4 OFFSET1:0

A baseline-only graphics system will leave these pins as no connects. A baseline/extended graphics system will see 03h on OFFSET1:0, which is the zero offset state, due to its pull-ups or the video system drive.

6.3.5 GENCLK

Undefined in baseline modes.

6.3.5 EGEN*

Undefined in baseline modes.

7.0 Extended Mode Operation and Requirements

P31:16, GRDY, VRDY, FSTAT, GENCLK, EGEN*, and OFFSET1:0 may be used to achieve functionality beyond the baseline requirements. This may include 32-bit transfers, multiple pixels per clock, YCrCb color space data, locking to NTSC video, and asynchronous video input to a FIFO on the graphics system.

Extended systems may be asynchronous (FIFO-based) designs. In these cases, video data may be transferred across the interface at any time, completely independent of the syncs, blanking and clocking controls generated by the graphics board. In this mode there is no requirement for a well-defined relationship between DCLK and VCLK. In general, pixels must be delivered by the video system in time for them to be consumed by the graphics system.

The GRDY signal is a transfer enable signal that may be used by the graphics board to request the transfer of video data early. For example, the display of YCrCb video data requires that 16 bits of video data be delivered one clock early in order to perform color space conversion. It is not practical to assume that the video pipeline and the graphics pipeline inside all DACs will be the same.
All extended 32 bit input modes are required to use the VRDY signal.

Extended mode functionality must be setup via a software driver provided by the graphics or video board vendor. No dedicated signals for configuration are present on the connector.

Because there exists a wide variety of multimedia extensions to operating systems, it is not within the scope of this standard to specify a single method of software configuration. Future VESA technical notes will make recommendations for configuring the interface for specific system environments.

In general, the software configuration mechanism must query both the video and graphics subsystems for their capabilities, i.e. 16/32 bit, multiplex modes supported, RGB or YCrCb color space support, etc., and then configure both sides of the connection for the highest level of compatibility that will deliver the highest quality video.

8.0 VAFC Pinout

Name	Pin #	Pin #	Name
RSRV0	1	41	GND
RSRV1	2	42	GND
GENCLK	3	43	GND
OFFSET0	4	44	GND
OFFSET1	5	45	GND
FSTAT	6	46	GND
VRDY	7	47	GND
GRDY	8	48	GND
BLANK*	9	49	GND
VSYNC	10	50	GND
HSYNC	11	51	GND
EGEN*	12	52	GND
VCLK	13	53	GND
RSRV2	14	54	GND
DCLK	15	55	GND
EVIDEO*	16	56	GND
P0	17	57	P1
GND	18	58	P2
P3	19	59	GND
P4	20	60	P5
GND	21	61	P6
P7	22	62	GND
P8	23	63	P9
GND	24	64	P10
P11	25	65	GND
P12	26	66	P13
GND	27	67	P14
P15	28	68	GND
P16	29	69	P17
GND	30	70	P18
P19	31	71	GND
P20	32	72	P21
GND	33	73	P22
P23	34	74	GND
P24	35	75	P25
GND	36	76	P26
P27	37	77	GND
P28	38	78	P29
GND	39	79	P30
P31	40	80	GND

9.0 Connector Recommendations

The VAFC connector is an 80-pin high density type utilizing .100 x .050 pin spacing. The connector is designed to use 0.025" spaced ribbon cable.

Manufacturer	Vertical PCB	Right Angle PCB	Ribbon Cable
AMP	2-557102-1	2-557100-1	557089-7
MOLEX	15-92-2080	71661-2080	15-92-3080

10.0 Pin Rules and Drive Levels

The following rules apply for pin drivers and receivers:

- Voltage levels are 0-3.3 volts to 0-5 volts - i.e. basic TTL input levels, TTL or CMOS drive.
- Direct ASIC drive is preferred over TTL buffers to control edge rates, skew, and reduce cost.
- It is recommended that DCLK and VCLK clock drivers are to be 8-12 ma ASIC cells to provide sufficient high speed drive without excessive ringing.
- Only one CMOS load maximum DCLK and VCLK fanout.
- Other drivers are 4-6 ma ASIC cells to provide sufficient drive without excessive ringing.
- DC drain >1ma/pin is not recommended despite the drive available.
- Recommended slew time is 1-2 ns, preferably driver controlled to limit undershoot and crosstalk. Overshoot and undershoot should be limited to 0.5 volt.
- Nominal 22 ohm source damping resistors are required on all high speed control pins. Actual value should be selected to ensure signal integrity.
- No destination termination is required or recommended.
- The VCLK input receivers are standard TTL level Schmitt inputs to eliminate false clocks due to reflections.
- Other receivers are standard TTL levels (Schmitt optional, not required).
- Cable impedance will be between 65 and 85-ohm when measured in a ground-signal-ground configuration.
- **All** grounds must be connected to ground at both ends, preferably to a ground plane.
- All high speed control signals are in a 1:1 ground sandwich for maximum signal integrity.
- All data pins have 2:1 grounds to reduce connector size.
- 2" maximum PCB trace length should be maintained between driver or receiver device and connector.

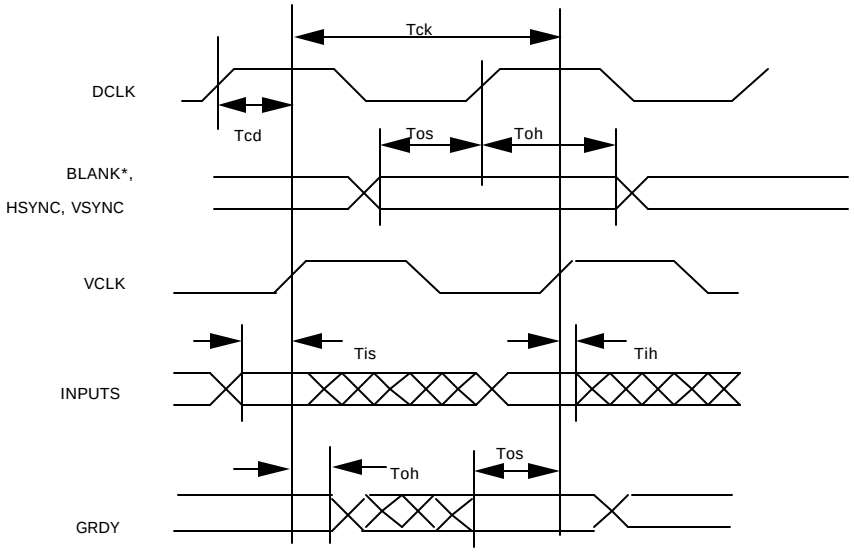
11.0 Timing

11.1 General Timing Notes

To account for effects of cable loading, all timing measurements are based on a fully connected system consisting of a graphics system and video system connected by a 7" ribbon cable.

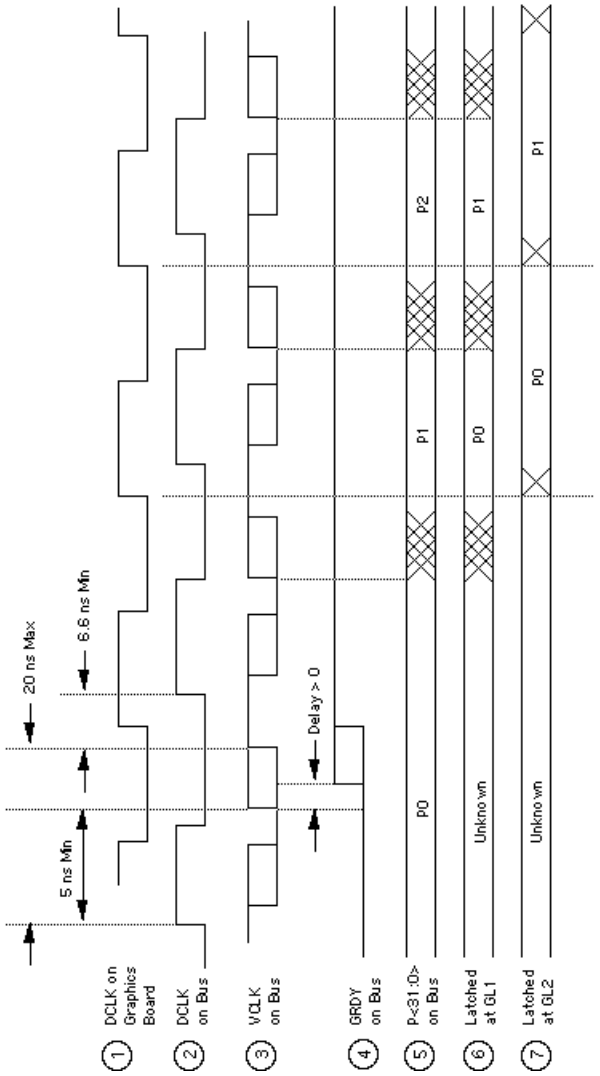
All signals have the following basic timing:

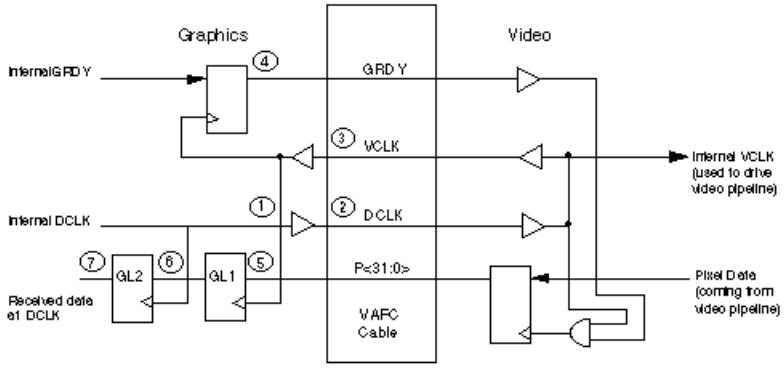
Tck	Clock period	26.6 ns min	This corresponds to 37.5 MHz max DCLK.
Tch	Clock high	10 ns min	
Tcl	Clock low	10 ns min	
Tos	Output setup	10 ns min	Data must be stable 10 ns before the clock edge.
Toh	Output hold	2 ns min	Data must hold for 2 ns after the clock edge.
Tis	Input setup	10ns min	Inputs must be stable 10 ns before the receiving clock edge.
Tih	Input hold	2ns min	Inputs must remain stable 2 ns after the receiving clock edge.
Tcd	DCLK to VCLK delay	5ns min 20ns max	For synchronous transfers, VCLK must meet this parameter.



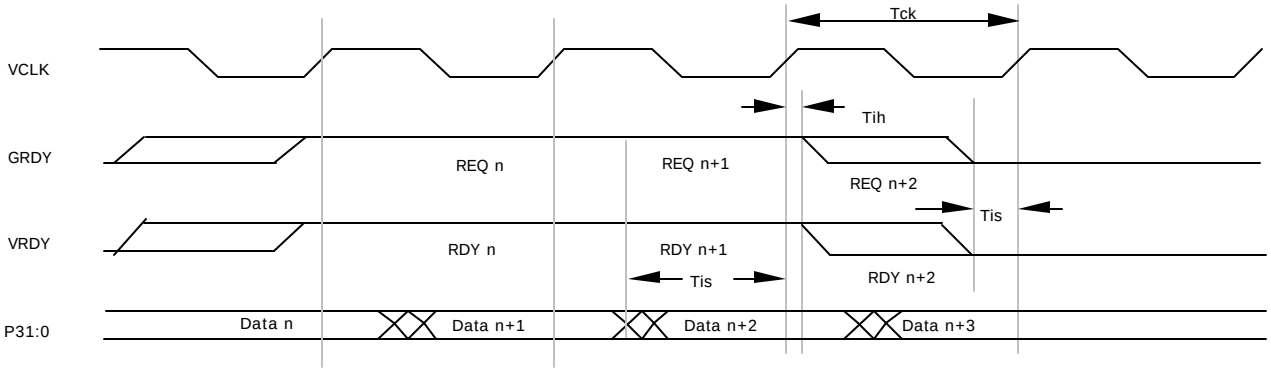
The maximum frequency for DCLK and VCLK are 37.5 MHz, or 75 MHz/2. This is based on 75 MHz as a standard VESA 1024x768 70 Hz mode. It may be possible to program a particular graphics or video controller combination to operate above this frequency, however correct operation is not guaranteed, and this is outside VESA compatibility.

11.2 Video Data Cycle - Input Modes

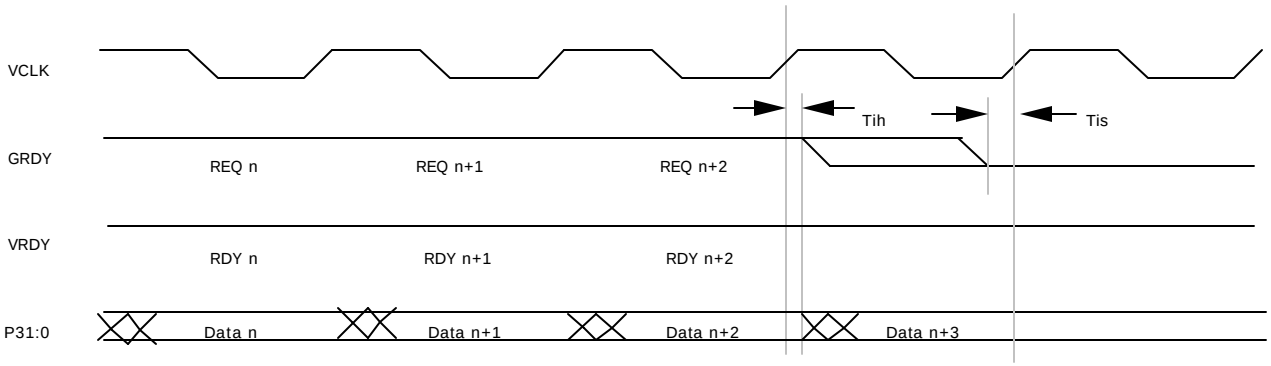




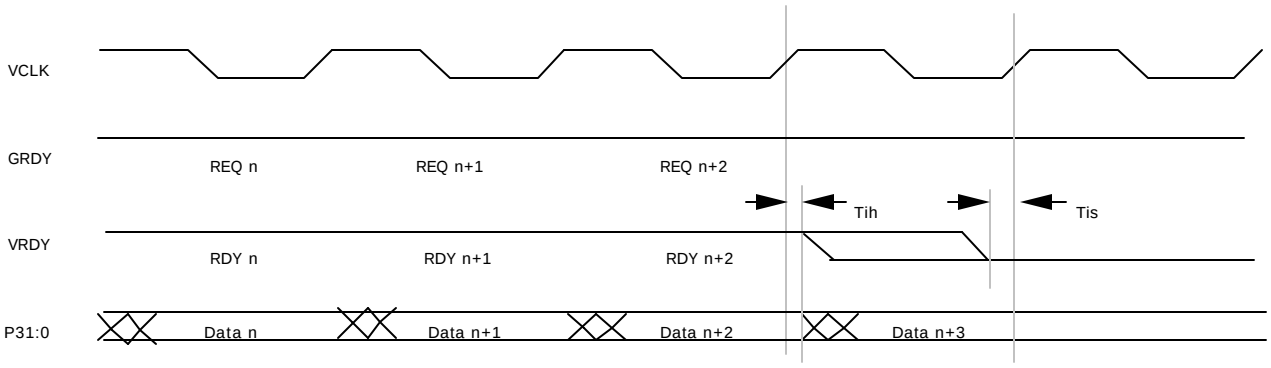
Video Input Timing



Three data requests, normal operation



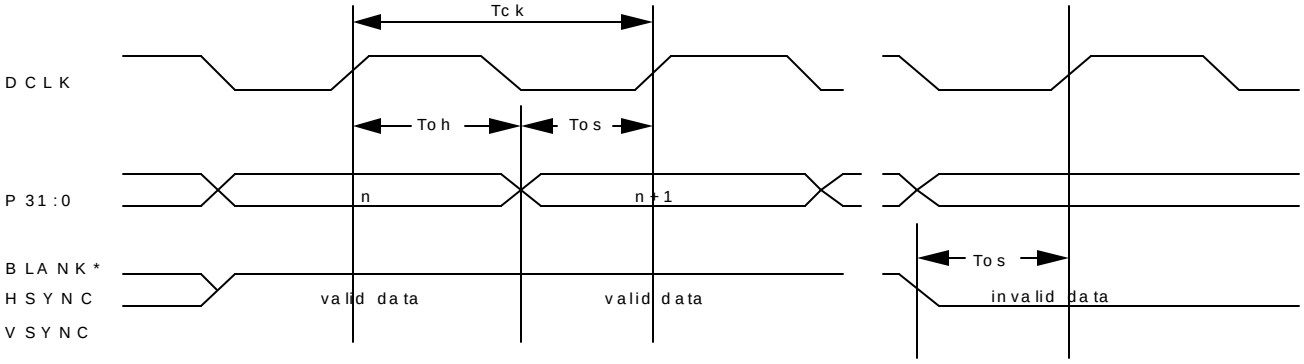
GRDY goes not ready



VRDY goes not ready

GRDY and VRDY must be sampled on the rising edge of VCLK. If either signal is not ready, the data on the P<31:0> bus at the time the signal went not ready must be held on the bus until both signals once again both go ready.

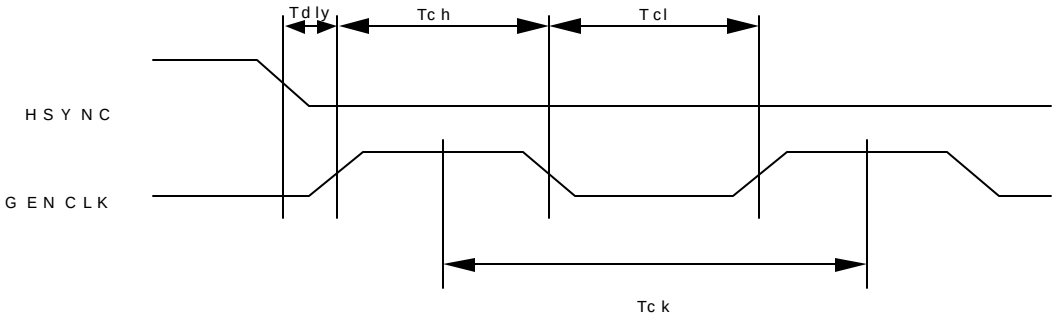
11.3 Video Data Transfer Cycle - Output Modes



In this mode, data is sent from the graphics board to the video board.

- DCLK is driven from the graphics source, typically a submultiple of the pixel clock
- BLANK* defines the display area
- Outside the valid data area, the DAC may send any data
- VRDY and GRDY are not used in output modes

11.4 Genlock Timing

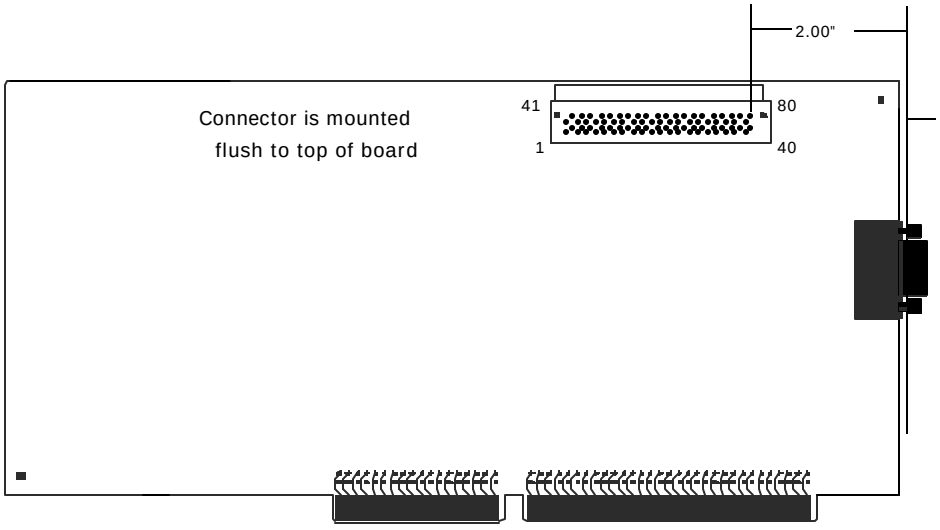


Tdly, the clock delay between the trailing edge of HSYNC and the leading edge of GENCLK, should be consistent from line to line to reduce jitter.

The maximum clock is 37.5MHz. The exact clock frequency is designed to be flexible, allowing either square pixels or various degrees of underscan or overscan.

12.0 Recommended Connector Orientation and Board Placement

The following diagram shows the recommended connector orientation and board placement for a typical ISA system. Similar placement is recommended for VL, MCA, PCI, ISA, and EISA cards. Placement is relative to the mounting bracket and the upper top right corner of the board.



Appendix A Related Documents/Other Organizations

VESA Standard VS890803 "VESA Standard VGA Pass-Through Connector"

IBM Publication "Personal System/2 Hardware Interface Technical Reference", first edition, May 1988

CCIR Recommendation 601, Document 11/1041-E, 11 December 1985

Appendix B Revision History

Revision 1.0 Added VESA logo. Replaced AOL reference with vesa-support@exodus.net in Support for this Specification. Revised style.