Preliminary Data Sheet
March 1992

AT&T Microelectronics

ATT20C491, 16M Color
ATT20C492, 256K Color
True-Color CMOS RAMDACs

Features

- 100/80/66/55 MHz operation
- 16M (256K), 64K, 32K, 256 on-screen colors
- Eight software selectable color modes:
  — 24- (18-), 16-, 15-bit gamma corrected true color
  — 24- (18-), 16-, 15-bit CLUT bypass true color
  — 8-bit pseudocolor
- True color eliminates color palette contention
- True color helps eliminate aliasing
- *XGA**, *TARGA*†, HICOLOR formats
- ATT20C492 powers down to 3 mA typical while retaining palette updates (ATT20C491)
- Automatically disables external V_{REF} during powerdown
- Signature analysis test register
- Low power dissipation 0.7 W typical
- Internal V_{REF} accuracy better than ±3%
- On-chip output comparators for monitor detection
- Antisparkle circuitry
- 8- or 6-bit DACs (492 = 6 bit only)
- 256 x 24 (18) color RAM
- 15 x 24 (18) overlay RAM
- RS-343A, RS-170, and *PS/2** compatible
- 44-pin PLCC industry-standard compatible footprints

Applications

- True-color add-in card or motherboard PC designs
- Display for high-color resolution image capture
- Laptop applications

* *PS/2* is a registered trademark and *XGA* is a trademark of International Business Machines Corporation.
† *TARGA* is a trademark of Truevision Corporation.
‡ *Microsoft Windows* is a registered trademark of Microsoft Corporation.

Description

The ATT20C491/492 CMOS RAMDACs support 24- (18-), 16-, 15-bit true color along with 8-bit pseudocolor applications. These devices also support 24- (18-), 16-, 15-bit true-color bypass for direct access to the DAC inputs without going through the color look-up table (CLUT) RAM. The ATT20C491/ 492 support *XGA*, *Microsoft Windows* ‡, *TARGA*, and HICOLOR graphics. The 491/492 ensure correct window colors for multiapplication displays. True color enables software to antialias by color dithering.

True-color graphics allow multiple applications simultaneous use of 16M colors. Multiple software applications no longer contend for control of 256 colors. Each application's window has the desired colors. True-color graphics helps eliminate aliasing by providing a full range of colors for each pixel. Each pixel in a stair-stepped diagonal line can be color blended with surrounding pixels to create a smooth diagonal line.

The ATT20C491 device is a 24-bit true-color upgrade and is pin and function compatible with the ATT20C477A/475A and the SC11488. The ATT20C492 is pin and function compatible with the SC11486. ATT20C492 is an ATT20C491 with 6-bit DACs, no powerdown, and no sync enable for individual R, G, B channels.

These devices include three 8-/6-bit video DACs with antisparkle circuitry. The ATT20C491/492 have on-chip comparators to detect connection to a monitor. An on-chip voltage reference is accurate to better than ±3%.

These devices are offered in the industry-standard 44-pin PLCC package and have a compatible footprint. It is designed to work with the internal or an external voltage reference only.

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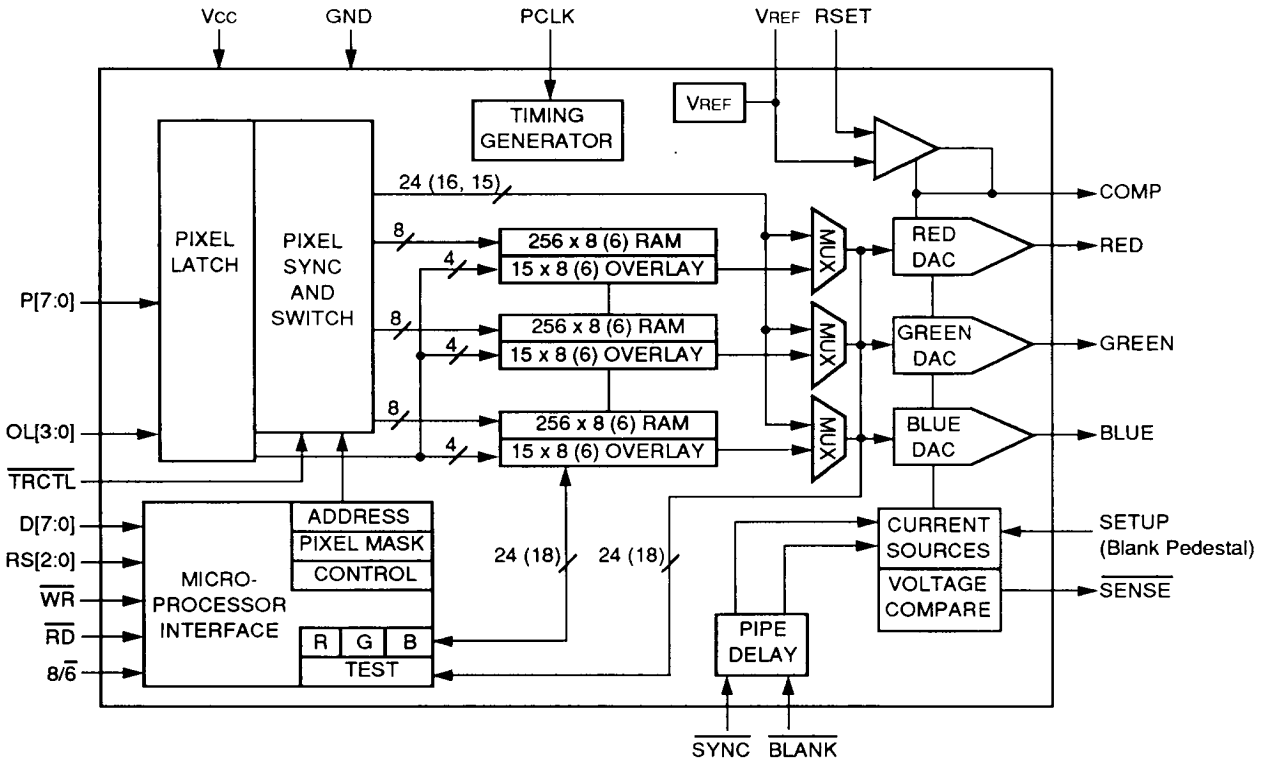


Figure 1. Block Diagram

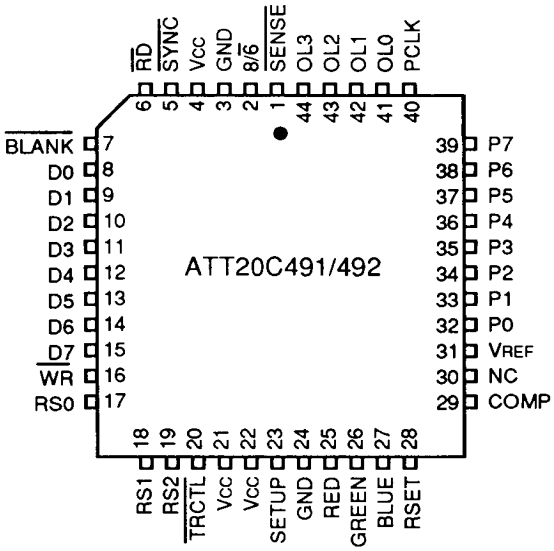


Figure 2. 44-Pin PLCC Pin Diagram

Pin Information

Table 1. Pin Descriptions

ATT20C491/492 Pin #	Symbol	Type	Name/Function
1	$\overline{\text{SENSE}}$	O	**$\overline{\text{SENSE}}$ (Active-Low).** TTL compatible. Monitor detection signal. $\overline{\text{SENSE}}$ is a logic 0 if one or more of the red, green, or blue outputs have exceeded the internal voltage reference level of 340 mV. $\overline{\text{SENSE}}$ may not be stable while SYNC is toggling.
2	8/ $\overline{6}$	I	**8/ $\overline{6}$.** TTL compatible. Color resolution select. This control input specifies whether the MPU is reading and writing 8 bits (logic 1) or 6 bits (logic 0) of color information each cycle. This pin is ORed with CR1 in the control register. On the ATT20C492, this pin has no internal connection, and the device is 6 bit only.
3, 24	GND	—	**Ground.**
4, 21, 22	Vcc	—	**Power.**
5	$\overline{\text{SYNC}}$	I	**$\overline{\text{SYNC}}$ (Active-Low).** TTL compatible. Latched on the rising edge of PCLK. $\overline{\text{SYNC}}$ removes a 7.62 mA (RS-343A) current source from each RGB output depending on the logic value of the color sync enable bits in the control register (CR[4:2]). For $\overline{\text{SYNC}}$ to operate properly, it should be asserted only during blanking. For systems having a sync signal separate from the RAMDAC, $\overline{\text{SYNC}}$ should be tied low to turn off the sync current source.
6	$\overline{\text{RD}}$	I	**Read (Active-Low).** TTL compatible. When $\overline{\text{RD}}$ is low, data transfers from the selected internal register to the data bus. RS[2:0] is latched on the falling edge of $\overline{\text{RD}}$.
7	$\overline{\text{BLANK}}$	I	**$\overline{\text{BLANK}}$ (Active-Low).** TTL compatible. $\overline{\text{BLANK}}$ is latched on the rising edge of PCLK. When $\overline{\text{BLANK}}$ is low, the 1.44 mA current source on the analog outputs will be turned off. The DACs ignore digital input from memory. The RAMDAC and overlay memory can be updated during blanking.
8—15	D[7:0]	I/O	**Data Bus.** TTL compatible. Data is transferred between the data bus and the internal registers under control of the $\overline{\text{RD}}$ / $\overline{\text{WR}}$ signals. In an MPU write operation, D[7:0] is latched on the rising edge of $\overline{\text{WR}}$. To read data D[7:0] from the device, $\overline{\text{RD}}$ must be in an active-low state. The rising edge of the $\overline{\text{RD}}$ signal indicates the end of a read cycle. Following the read cycle, the data bus will go to a high-impedance state. For 6-bit operation, color data is contained in the lower 6 bits of the data bus. D0 is the LSB, and D5 is the MSB. When the MPU writes color data, D6 and D7 are ignored. During MPU read cycles, D6 and D7 are a logic 0. The ATT20C492 is 6 bit only.
16	$\overline{\text{WR}}$	I	**Write (Active-Low).** TTL compatible. $\overline{\text{WR}}$ controls the data transfer from the data bus to the selected internal register. D[7:0] data is latched at the rising edge of $\overline{\text{WR}}$, and RS[2:0] data is latched at the falling edge of $\overline{\text{WR}}$.
17—19	RS[2:0]	I	**Register Select.** TTL compatible. These inputs are sampled on the falling edge of the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ to determine which one of the internal registers is to be accessed. RS2 is not needed to access the control register. See the Control Register section under Functional Description.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

ATT20C491/492 Pin #	Symbol	Type	Name/Function
20	$\overline{\text{TRCTL}}$	I	**True Control.** TTL compatible. This input determines whether the control register or the overlay inputs select the color mode. If a logic high, control register bits CR[7:5] set the color mode. If a logic low, the OL[3:0] inputs select the color mode. See Tables 3 and 4 for color modes.
23	SETUP	I	**SETUP.** TTL compatible. A logic high will cause a blanking pedestal of 1.44 mA on an RS-343A output.
25 26 27	RED GREEN BLUE	O	**Color Signals.** These pins are analog outputs. These high-impedance current sources are capable of driving a double-terminated 75 Ω coaxial cable.
28	RSET	I	**Reference Resistor.** An external resistor (RSET) is connected between the RSET pin and GND to control the magnitude of the full-scale current. Refer to DAC Gain section under Functional Description.
29	COMP	—	**Compensation Pin.** Bypass this pin with an external 0.1 µF capacitor to V_{CC}.
30	NC	—	**No Connect.** No internal connection to the chip.
31	V_{REF}	I	**Voltage Reference.** If an external voltage is used, supply this input with a 1.235 V reference.
32—39	P[7:0]	I	**Pixel Address.** TTL compatible. These pins are latched on the rising edge of PCLK except in HICOLOR1 mode when they are latched with both the rising and falling edges of PCLK. Pixels can be presented to the DACs as color data or used as addresses to look up color data in the color RAM. Unused inputs should be connected to GND.
40	PCLK	I	**Pixel Clock.** TTL compatible. The duty cycle of the clock should be between 30% and 70%. The rising edge of the pixel clock latches the pixel address and $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ inputs. The pixel clock controls the four- or eight-stage video pipelined operation.
41—44	OL[3:0]	I	**Overlay Address.** TTL compatible. These pins are latched on the rising edge of PCLK. These inputs are used to specify one of the 15 addresses of the color overlays. When the overlay address is non-zero, the pixel address inputs are ignored. Unused inputs should be connected to GND. If $\overline{\text{TRCTL}}$ is low, these pins determine the color mode. A change to these pins requires four (bypass modes) or eight (LUT modes) pixel clocks before the new color mode is valid.

Table 2. Control Input Truth Table

RS2	RS1	RS0	Addressed by the MPU
0	0	0	Address register (RAM write mode)
0	1	1	Address register (RAM read mode)
0	0	1	RAMDAC RAM
0	1	0	Pixel read mask register
1	0	0	Address register (overlay write mode)
1	1	1	Address register (overlay read mode)
1	0	1	Overlay registers (test register)
1	1	0	Control register

Functional Description

The following tables detail the eight color modes of the ATT20C491/492. These modes are set by bits CR[7:5] of the control register or by the overlay input pins OL[3:1]. If TRCTL is low, the overlay inputs overide the color mode bits in the control register.

Table 3. Control Register Controls Color Mode ($\overline{\text{TRCTL}}$ = High)

						DAC Inputs			
Mode	**CR [7:5]**	**Description**	**Clock Edges**	**Gamma Corrected**	**Pipe Delay**	**R[7:0]**	**G[7:0]**	**B[7:0]**	**Comment**
0	000	8-bit pseudocolor	1	Yes	4	P[7:0]	P[7:0]	P[7:0]	Default
1	001	15-bit true color	2	Yes	8	P[14:10] rrrrr000	P[9:5] ggggg000	P[4:0] bbbbb000	—
2	010	24- (18-)bit true color	3	Yes	8	P[23:16] rrrrrrrr	P[15:8] gggggggg	P[7:0] bbbbbbbb	—
3	011	16-bit true color	2	Yes	8	P[15:11] rrrrr000	P[10:5] gggggg00	P[4:0] bbbbb000	—
4*	100	15-bit bypass	1	No	4	P[14:10] rrrrr000	P[9:5] ggggg000	P[4:0] bbbbb000	HICOLOR1
5	101	15-bit bypass	2	No	4	P[14:10] rrrrr000	P[9:5] ggggg000	P[4:0] bbbbb000	HICOLOR2
6	110	16-bit bypass	2	No	4	P[15:11] rrrrr000	P[10:5] gggggg00	P[4:0] bbbbb000	*XGA2*
7	111	24- (18-)bit bypass	3	No	4	P[23:16]	P[15:8]	P[7:0]	—

Table 4. Overlay Inputs Control Color Mode ($\overline{\text{TRCTL}}$ = Low)

						DAC Inputs			
Mode	**OL [3:1]**	**Description**	**Clock Edges**	**Gamma Corrected**	**Pipe Delay**	**R[7:0]**	**G[7:0]**	**B[7:0]**	**Comment**
0	000	8-bit pseudocolor	1	Yes	4	P[7:0]	P[7:0]	P[7:0]	Default
1	001	15-bit true color	2	Yes	8	P[14:0] rrrrr000	P[9:5] ggggg000	P[4:0] bbbbb000	—
2	010	24- (18-)bit true color	3	Yes	8	P[23:16] rrrrrrrr	P[15:8] gggggggg	P[7:0] bbbbbbbb	—
3	011	16-bit true color	2	Yes	8	P[15:11] rrrrr000	P[10:5] gggggg00	P[4:0] bbbbb000	—
4*	100	15-bit bypass	1	No	4	P[14:10] rrrrr000	P[9:5] ggggg000	P[4:0] bbbbb000	HICOLOR1
5	101	15-bit bypass	2	No	4	P[14:10] rrrrr000	P[9:5] ggggg000	P[4:0] bbbbb000	HICOLOR2
6	110	16-bit bypass	2	No	4	P[15:11] rrrrr000	P[10:5] gggggg00	P[4:0] bbbbb000	*XGA2*
7	111	24- (18-)bit bypass	3	No	4	P[23:16]	P[15:8]	P[7:0]	—

* This mode is valid up to 66 MHz.

Functional Description (continued)

Table 5. Control Register

This register is operational on powerup. It can be read or written to by the MPU at any time and is not initialized.

Bit	Name/Description
CR[7:5]	**Color Mode.** These bits are used to control the various color modes as shown in Tables 3 and 4. These bits are active when TRCTL is logic high.
CR[4:2]	**Sync Enable (ATT20C491 only).** Logic 0: Sync disabled. Logic 1: Sync enabled. Bits CR4, CR3, and CR2, respectively specify whether the blue, green, or red outputs will have sync offset current. A logic 1 specifies sync current. The sync currents enabled by CR4, CR3, and CR2 are controlled by the SYNC pin. For noncomposite sync, tie the SYNC pin to logic 0. For the ATT20C492, SYNC is enabled for the red, green, and blue outputs at all times.
CR1	**8-/6-bit Select (ATT20C491 only).** Logic 0: 6 bit. Logic 1: 8 bit. A logic 1 specifies 8-bit color operation (16M possible colors). A logic 0 specifies 6-bit color operation (256K possible colors). This bit is ORed with the 8/ 6 pin. The ATT20C492 has 6-bit operation only.
CR0	**Sleep Enable (ATT20C491 only).** Logic 0: Normal operation. Logic 1: Sleep mode. If this bit is logic 0, the device will be in normal operation. If this bit is logic 1, the DAC is turned off and the palette RAM is powered down. The RAM retains data and will wake up to accept inputs from the MPU port. After accepting MPU data, the RAM returns to the sleep state. After programming the device for normal operation, valid data will appear at the DAC outputs in about one second. This bit is reserved in the ATT20C492, and the device works in normal operation only.

Functional Description (continued)

Color Modes

The ATT20C491/492 provides eight different color modes that are selectable by programming the MPU control register bits CR[7:5]. Modes designated as bypass do not make use of the color look-up tables or pixel read mask registers. Overlays take precedence in color modes using the color look-up tables. In LUT bypass modes, the overlay inputs are ignored. In modes with multiple clocks per pixel, a pixel modulo 2 or 3 counter will provide the internal load pulse that updates the CLUT address registers. An active $\overline{\text{BLANK}}$ signal clears the modulo counter. For modes 0—3, note that gamma correction data in the ATT20C492 LUT must be input on the lower 6 bits of D[7:0]. The six LSBs D[5:0] will be shifted to the six MSBs in the color RAM. The blue pixel is latched first, followed by green and red. The BGR sequence continues until $\overline{\text{BLANK}}$ goes low. The following are explanations of each color mode:

Mode 0: 8-bit pseudocolor (one clock per pixel). This mode is selected by setting control register bits CR[7:5] to 000 with $\overline{\text{TRCTL}}$ held high, or by setting overlay inputs OL[3:1] to 000 with $\overline{\text{TRCTL}}$ low. In this mode, 8 bits of pixel address are input to the device on every video clock cycle. The P[7:0] inputs are latched on every rising edge of the pixel clock. (See Figure 3.)

Mode 1: 15-bit true color (5-5-5 two clocks per pixel). This mode is selected by setting the control register bits CR[7:5] to 001 with $\overline{\text{TRCTL}}$ held high, or by setting overlay inputs OL[3:1] to 001 with $\overline{\text{TRCTL}}$ low. Each look-up table (red, green, and blue) is presented with 5 bits of pixel address. This pixel address bits are collected over two rising edges of the pixel clock. $\overline{\text{BLANK}}$ going high will signal that the first pixel address bits are available on P[7:0]. The rising edge of PCLK that captures $\overline{\text{BLANK}}$ going high also captures the LSBs of the pixel address. The LSBs are latched first, followed by the MSBs. The LSBs and MSBs follow in succession until $\overline{\text{BLANK}}$ goes low. The latched 16-bit field is partitioned as follows: bits 14:10 form the red pixel address; 9:5, the green; and 4:0, the blue (bit 15 is ignored). See Figures 3 and 4. The LSBs of the pixel LUT address are set to logic 0. In this mode, the DAC outputs will be updated on every second video clock.

Mode 2: 24-bit true color (three clocks per pixel). This mode is selected by setting the control register bits CR[7:5] to 010 with $\overline{\text{TRCTL}}$ held high, or by setting overlay pins OL[3:1] to 010 with $\overline{\text{TRCTL}}$ held low. Each look-up table is presented with an 8-bit address. The pixel information is collected over three rising edges of the pixel clock. $\overline{\text{BLANK}}$ going high captures the blue pixel LUT address. (See Figure 3.) In this mode, the DAC outputs will be updated on every third video clock. The ATT20C492 displays 256K colors (18 bits) in this mode.

Mode 3: 16-bit true color (5-6-5 two clocks per pixel). This mode is selected by setting the control register bits CR[7:5] to 011 with $\overline{\text{TRCTL}}$ held high, or by setting overlay inputs OL[3:1] to 011 with $\overline{\text{TRCTL}}$ low. Each look-up table (red, green, or blue) is presented with 5 or 6 bits of pixel address. The pixel address is collected over two rising edges of the pixel clock. $\overline{\text{BLANK}}$ going high will signal that the first pixel address bits are available on P[7:0]. The rising edge of PCLK that captures $\overline{\text{BLANK}}$ going high also captures the LSBs of the pixel address. The LSBs are latched first, followed by the MSBs. The LSBs and MSBs follow in succession until $\overline{\text{BLANK}}$ goes low. The latched 16-bit field is partitioned as follows: bits 15:11 form the red pixel data; 10:5, the green; and 4:0, the blue. (See Figures 3 and 4.) The LSBs of the pixel LUT address are set to logic 0. In this mode, the DAC outputs will be updated on every second video clock.

Mode 4: 15-bit true-color bypass (5-5-5 one clock per pixel). This mode corresponds to Sierra Semiconductor 15-bit HICOLOR1 mode. It is selected by setting the control register bits CR[7:5] to 100 with $\overline{\text{TRCTL}}$ held high, or by setting overlay inputs OL[3:1] to 100 with $\overline{\text{TRCTL}}$ low. The pixel information is collected over a single pixel clock cycle. The rising edge of PCLK latches the eight LSBs followed by the falling edge latching the eight MSBs. The latched 16-bit field is partioned as follows: bits 14:10 form the red pixel data; 9:5, the green; 4:0, the blue; and bit 15 is ignored. (See Figures 3 and 4.) The LSBs of the partitioned pixel information are set to logic 0. In this mode, the DAC outputs will be updated on every video clock.

Functional Description (continued)

Color Modes (continued)

Mode 5: 15-bit true-color bypass (5-5-5 two clocks per pixel). This mode is selected by setting the control register bits CR[7:5] to 101 with TRCTL held high, or by setting overlay inputs OL[3:1] to 101 with TRCTL low. The pixel information is collected over two rising edges of the pixel clock. BLANK going high will signal that the first pixel information is available on P[7:0] The rising edge of PCLK that captures BLANK going high also captures the LSBs of the pixel information. The LSBs are latched first, followed by the MSBs. The LSBs and MSBs follow in succession until BLANK goes low. The latched 16-bit field is partioned as follows: bits 14:10 form the red pixel data; 9:5, the green; 4:0, the blue; and bit 15 is ignored. (See Figures 3 and 4.) The LSBs of the pixel information are set to logic 0. In this mode, the DAC outputs will be updated on every second video clock.

Mode 6: 16-bit true-color bypass (5-6-5 two clocks per pixel). This mode is selected by setting the control register bits CR[7:5] to 110 with TRCTL held high, or by setting overlay inputs OL[3:1] to 110 with TRCTL low. The pixel information is collected over two rising edges of the pixel clock, and then is presented directly to the DACS.

BLANK going high will signal that the first pixel information is available on P[7:0]. The rising edge of PCLK that captures BLANK going high also captures the LSBs of the pixel information. The LSBs are latched first, followed by the MSBs. The LSBs and MSBs follow in succession until BLANK goes low. The latched 16-bit field is partioned as follows: bits 15:11 form the red pixel data; 10:5, the green; and 4:0, the blue. (See Figures 3 and 4.) The LSBs of the pixel information are set to logic 0. In this mode, the DAC outputs will be updated on every second video clock. This is the *XGA2* mode.

Mode 7: 24-bit true-color bypass (three clocks per pixel). This mode is selected by setting the control register bits CR[7:5] to 111 with TRCTL held high, or by setting overlay inputs OL[3:1] to 111 with TRCTL low. The pixel information is collected over three rising edges of the pixel clock. BLANK going high will signal that the first pixel information is available on P[7:0]. The rising edge of PCLK that captures BLANK going high also captures the blue information of the first pixel. The blue pixel is latched first, followed by the green and red. Blue, green, and red follow in succession until BLANK goes low. (See Figure 3.) In this mode, the DAC outputs will be updated on every third video clock. The ATT20C492 displays 256K colors (18 bits) in this mode.

Table 6. Maximum Resolution by Speed Grade and Color Modes

CLKS	Mode No.	Mode	55 MHz	Clock Rate (MHz)	66 MHz	Clock Rate (MHz)	80 MHz	Clock Rate (MHz)	100 MHz	Clock Rate (MHz)
One	0	8-bit pseudo-color	800 x 600 72 Hz	50	1024 x 768 60 Hz	65	1024 x 768 75 Hz	80	1024 x 1024 60 Hz	95
	4	15-bit bypass	800 x 600 72 Hz	50	1024 x 768 60 Hz	65	—	—	—	—
Two	1	15-bit true color	640 x 480 60 Hz	50.35	640 x 480 72 Hz	62.4	800 x 600 60 Hz	80	800 x 600 72 Hz	100
	3	16-bit true color								
	5	15-bit bypass								
	6	16-bit bypass								
Three	2	24-, (18-) bit true color	640 x 480 43 Hz Interlace	54.78	—	—	640 x 480 60 Hz	75.5	640 x 480 72 Hz	93.6
	7	24-, (18-) bit bypass								

Functional Description (continued)

Color Modes (continued)

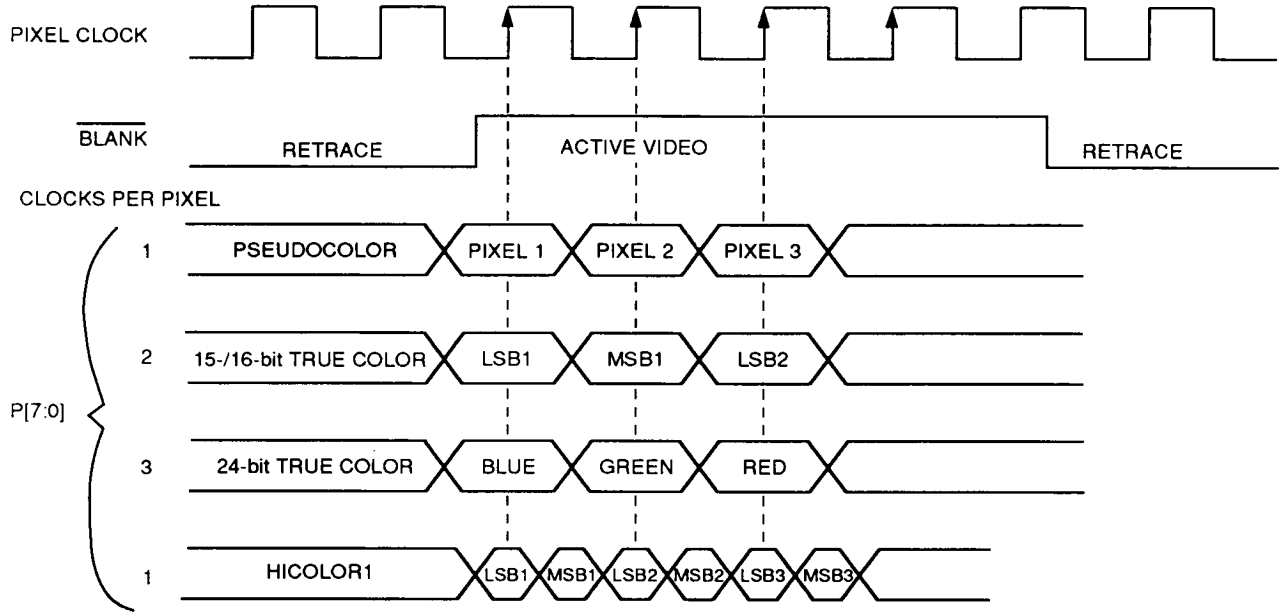
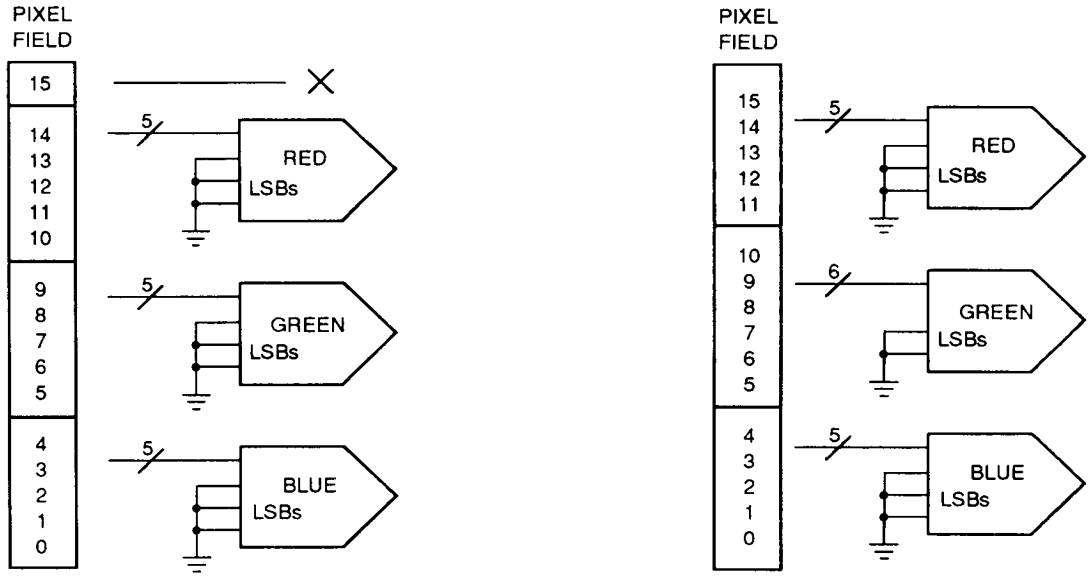


Figure 3. Pixel Data for Color Modes



A. 15-bit True Color (5-5-5) **B. 16-bit True Color (5-6-5)**

Figure 4. 15-/16-bit Field Split for Bypass Modes

Functional Description (continued)

Color Modes (continued)

Overlay Control

When $\overline{\text{TRCTL}}$ is low, the overlay pins OL[3:1] select the color mode. The color mode setting in the control register is ignored. OL3 corresponds to control register bit CR7, OL2 to CR6, and OL1 to CR5. While $\overline{\text{TRCTL}}$ is low, the overlay registers are disabled but still may be written by the MPU. If $\overline{\text{TRCTL}}$ is high (logic 1), the control register selects the color mode.

Overlays

Overlays take precedence over pixel information. Overlays are enabled in pseudo- and true-color modes, and are disabled in true-color bypass modes.

To display one of the 15 overlay colors, present the 4-bit value to the overlay port for one rising clock edge for pseudocolor and HICOLOR1, two rising clock edges for 15-/16-bit true color, or three rising clock edges for 24-bit true color. To change the overlay color for two and three clock modes, present a different 4-bit value or a zero value for one of the rising edges. A zero value will cause the DAC output color to be switched to the pixel color for 1/2 pixel for a two-clock mode and 1/3 pixel for a three-clock mode. (See Figure 5.)

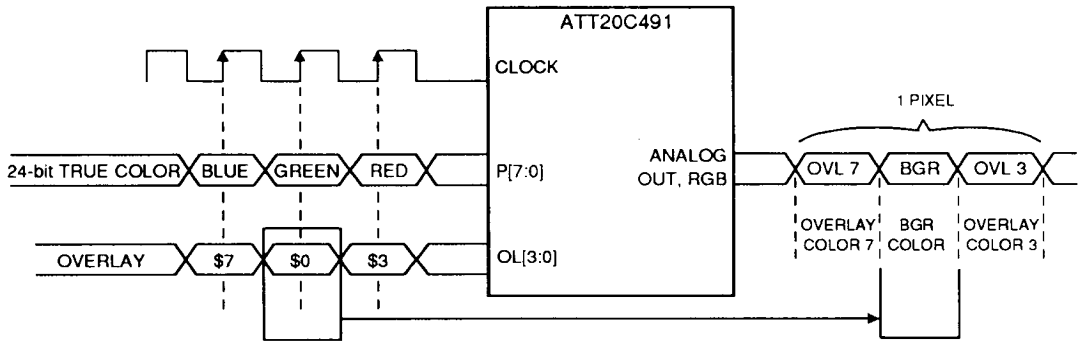


Figure 5. Overlay Color Operation in True-Color Modes

Functional Description (continued)

Internal Registers

Control Register

The control register can be written to or read by the MPU at any time and is not initialized. CR0 is the least significant bit in the control register and corresponds to D0 of the MPU port. Table 5 defines the bits of the control register. Bits CR[7:5] determine the color mode when TRCTL is a logic 1, as shown in Tables 3 and 4. Bits CR[4:2] indicate which analog channels will have composite sync information. Sync will be present on the RGB channels selected when SYNC is asserted. CR1 controls the color resolution by configuring the RAMDAC for 8-bit (16.8M colors) or 6-bit (262K colors) operation. This bit is logically ORed with the 8/6 pin. A logic 1 in bit CR0 puts the RAMDAC to sleep. The RAMDAC wakes up to accept updates to the color RAM, then goes back to sleep. In this manner, the device tracks changes to the color look-up table while utilizing minimum power.

Alternate Control Register Access

For graphics systems controllers that do not have a control signal for RS2, the control register may be accessed by using the following sequence. A flag will be set when the pixel read mask register (RS1 = 1, RS0 = 0) is read four times consecutively. The next read or write to the pixel mask register will be sent to the control register. In this manner, any of the eight color modes may be selected with bits CR[7:5]. Reading or writing any other register than the pixel read mask register will reset the flag. After accessing the control register, the flag is reset.

Pixel Read Mask Register

The contents of the pixel read mask register may be accessed by the MPU at any time and is not initialized. The read mask register bits are logically ANDed with the 8-bit pixels. A logic 1 stored in a data bit of the read mask register leaves the corresponding bit in the pixel unchanged. A logic 0 in the read mask register sets the pixel bit to zero. Bit D0 of the pixel read mask register corresponds to pixel bit P0.
In bypass modes, pixels are not modified by the read mask register. Bit D0 of the pixel read mask register corresponds to pixel bit P0 (pseudocolor), bit B0 and G3 of a 16-bit field (15-/16-bit true color), or B0, G0, and R0 (24-bit true color).

Test Register

A signature analysis circuit accumulates pixels. The signature analysis is made available through the overlay register 0. The test register provides video speed testing of the pixel path for the various color modes. These three 8-bit registers accumulate a signature based on an initial seed value and the value of the incoming pixels in any color mode. A fixed seed value of $AA will be written to each red, green, and blue test register by writing any color value to overlay 0. The signature is accumulated when BLANK goes high and stops when BLANK goes low.

The accumulated value of the test registers can be read by doing three consecutive reads to the overlay address 0 to get the red, green, and blue signatures. Access to this register is limited to blanking intervals only.

MPU Interface

The ATT20C491/492 supports a standard MPU interface, allowing the MPU direct access to the RAMDAC RAM, overlay color registers, or control register (see Figure 1). As outlined in Table 2, the RS[2:0] select inputs indicate whether the MPU is accessing the address register, RAMDAC RAM, overlay registers, read mask register, or control register. To eliminate the requirement for external address multiplexers, the 8-bit address register is used to address the RAMDAC RAM and overlay registers. ADDR0 corresponds to D0 and is the least significant bit.

Writing the RAMDAC

The MPU writes the address register (RAM write mode) with the address of the RAMDAC RAM location to be modified. Using RS[2:0] to select the RAMDAC RAM, the MPU completes three continuous write cycles (6 or 8 bits each of red, green, and blue). Following the blue write cycle, the 3 bytes of color information are concatenated into an 18- or 24-bit word and written to the location specified by the address register. The address register advances to the next location, which the MPU can modify by simply writing another sequence of red, green, and blue data. A block of color values in successive locations can be written to by writing the start address and performing continuous R, G, and B write cycles until the entire block has been written.

Functional Description (continued)

Reading the RAMDAC

The MPU loads the address register (RAM read mode) with the address of the RAMDAC RAM location to be read. The contents of the RAMDAC RAM at the specified address are copied into the RGB register, and the address register advances to the next RAM location. Using RS[2:0] to select the RAMDAC RAM, the MPU completes three continuous read cycles (6 or 8 bits each of red, green, and blue). After the blue read cycle, the contents of the RAMDAC RAM at the address specified by the address register are copied into the RGB registers, and the address register advances to the next address. A block of color values in successive locations can be read by writing the start address and performing continuous R, G, and B read cycles until the entire block has been read.

Writing the Overlay Registers

The MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. Using RS[2:0] to select the overlay registers, the MPU completes three continuous write cycles (6 or 8 bits each of red, green, and blue). Following the blue write cycle, the 3 bytes of color information are concatenated into an 18- or 24-bit word and written to the overlay location specified by the address register. The address register then advances to the next location, which the MPU can modify by simply writing another sequence of red, green, and blue data. A block of color values in successive locations can be written to by writing the start address and performing continuous R, G, and B write cycles until the entire block has been written.

Reading the Overlay Registers

The MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB register, and the address register advances to the next overlay location. Using RS[2:0] to select the overlay registers, the MPU completes three continuous read cycles (6 or 8 bits each of red, green, and blue).

After the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers, and the address register advances to the next address. A block of color values in successive locations can be read by writing the start address and performing continuous R, G, and B read cycles until the entire block has been read.

Additional Information

Following a blue read or write cycle to RAM location $FF, the address register resets to $00.

The four most significant bits of the address register ADDR[7:4] are ignored while accessing the overlay color registers. The MPU interface operates asynchronously to the pixel clock. Internal logic synchronizes data transfers between the RAMDAC RAM/overlay registers and the R, G, B color sub-register.

As a result, the $\overline{WR}$ and $\overline{RD}$ signals must maintain a logic high for several clock cycles. See Table 17 for $\overline{RD}$ and $\overline{WR}$ high time for further information. To eliminate sparkling on the CRT screen during MPU access to the RAMDAC RAMs, internal logic maintains the previous output color data on the analog outputs, while the transfer between look-up table RAMs and the RGB registers occurs.

To monitor the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 7. They are reset to 0 when the MPU writes to the address register, and are not reset to 0 when the MPU reads the address register. The MPU does not have access to these bits.

The other 8 bits of the address register ADDR[7:0], incremented following a blue read or write cycle, are accessible to the MPU and are used to address RAMDAC RAM locations and overlay registers, as outlined in Table 8.

The MPU can read the address register at any time without modifying its contents or the existing read/write mode. Note that the pixel clock must be active for MPU accesses to the RAMDAC RAM.

Functional Description (continued)

Additional Information (continued)

Table 7. Modulo Counter Operation

Value	Addressed by MPU
00	red value
01	green value
10	blue value

Table 8. Address Register (ADDR) Operation

RS2	RS1	RS0	Address	Addressed by MPU
0	0	1	$00–$FF	RAMDAC RAM
1	0	1	$X0	test register
1	0	1	$X1	overlay color 1
:	:	:	:	:
1	0	1	$XF	overlay color 15

8-/$\overline{6}$-bit Color Resolution

The 8/$\overline{6}$ pin and the 8/$\overline{6}$ bit in the control register (CR1) determine whether the MPU port reads and writes 6 or 8 bits of color data to the color look-up table RAM. The 8/$\overline{6}$ pin and the 8/$\overline{6}$ control register bit are logically ORed. In 6-bit mode, color data is on the lower 6 bits of the data bus, with D0 being the LSB and D5, the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logic 0. Note that in the 6-bit mode, the full-scale output current will be about 1.5% lower than when in the 8-bit mode. This is a result of the two LSBs of each 8-bit DAC always being a logic 0 in the 6-bit mode. In the 8-bit color mode, bit D0 is the color data LSB and bit D7 is the MSB.

Pixel and Overlay Pins

Table 9 outlines how the P[7:0] and OL[3:0] inputs address the RAMDAC RAM and overlay registers. The contents of the pixel read mask register can be accessed by the MPU at any time and are bit-wise logically ANDed with the P[7:0] inputs (LUT modes when TRCTL is high). Bit D0 of the pixel read mask register corresponds to pixel input P0. The LUT location pointed to by the pixel data provides 18 bits of color information to the three DACs in the 6-bit mode and 24 bits in the 8-bit mode.

To maintain synchronization with color data, the rising edge of the clock latches the SYNC and BLANK inputs. SYNC and BLANK add appropriately weighted currents to the analog outputs to produce the SYNC and BLANK pedestal currents as shown in Figures 6, 7, and 8 and Tables 11, 12, and 13.

The analog outputs are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

Table 9. Pixel and Overlay Control Truth Table

(Condition: Pixel Read Mask Register = $FF)

OL[3:0]	P[7:0]	Addressed by Frame Buffer
$0	$00	RAMDAC RAM location $00
$0	$01	RAMDAC RAM location $01
:	:	:
$0	$FF	RAMDAC RAM location $FF
$1	$XX	overlay color 1
:	$XX	:
$F	$XX	overlay color 15

Powerdown

The SLEEP command bit controls the powerdown. The device operates normally while the sleep bit is a logic 0. A logic 1 in the command register SLEEP bit turns off power to the RAM and the DACs. The RAM still retains the data and can still be read or written to while sleeping, as long as the pixel clock is running. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is completed.

The ATT20C491 disables all references both internal and external to the device, preventing current from flowing out of the device during powerdown. The internal reference disable circuitry eliminates the need for external disable logic and allows minimum power dissipation during sleep mode, regardless of the referencing scheme used.

Functional Description (continued)

$\overline{\text{SENSE}}$ Output

$\overline{\text{SENSE}}$ is a logic 0 if one or more of the red, green, or blue outputs have exceeded the internal voltage reference level (340 mV). This output is used to determine the presence of a CRT monitor, and, via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 340 mV reference has a ±40 mV tolerance. Note that $\overline{\text{SYNC}}$ should be a logic 0 for $\overline{\text{SENSE}}$ to be stable. When using the ATT20C491 in a socket of an earlier, compatible device, make sure that the $\overline{\text{SENSE}}$ pin is not tied to power or ground.

DAC Gain

The device gain from the voltage reference to the DAC output current is shown below. To set the full-scale white current on the DACs while using an internal or external voltage reference, use the formula below. V_{REF} is the voltage reference in volts, K is the gain constant from Table 9, and RSET is the resistor connected between the RSET pin and ground. Find the recommended RSET in Table 10.

I_{OUT} (mA) = [V_{REF} (V) * 1,000 * K] / RSET (Ω)

In this case, a voltage reference of 1.235 V with RSET = 147 Ω and a K factor of 3.17 results in I_{OUT} = 26.63 mA. A 6-bit DAC with no sync or blank results in a K factor of 2.1 and I_{OUT} = 17.64 mA.

As shown in Table 10, the recommended RSET for RS-343A compatibility applications (doubly terminated 75 Ω) is 147 Ω. The recommended RSET for *PS/2* applications (50 Ω) is 182 Ω.

Table 10. I_{OUT} Current

Output Waveform Level	RS-343A	*PS/2*	K Factor
Black to White (6 bit)	17.6 mA	14.25 mA	2.1
Black to White (8 bit)	17.6 mA	14.25 mA	2.125
Black to $\overline{\text{BLANK}}$	1.4 mA	—	0.1667
$\overline{\text{BLANK}}$ to $\overline{\text{SYNC}}$	7.6 mA	6.1 mA	0.9
Recommended RSET	147 Ω	182 Ω	—

Functional Description (continued)

DAC Gain (continued)

NO $\overline{\text{SYNC}}$		$\overline{\text{SYNC}}$	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

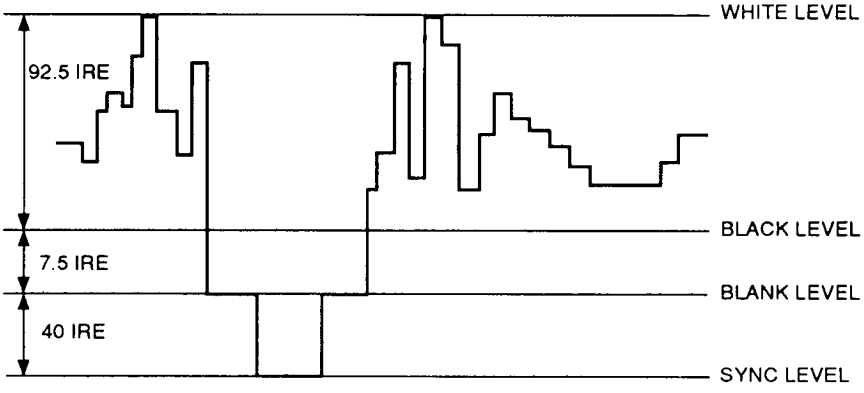


Figure 6. RS-343A Composite Video Output Waveforms

Table 11. RS-343A Video Output Truth Table (blank offset current to equal 7.5 IRE)

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	I_{OUT} (mA) $\overline{\text{SYNC}}$ Disabled	I_{OUT} (mA) $\overline{\text{SYNC}}$ Enabled
$FF	1	1	WHITE	19.05	26.67
data	1	1	DATA	data + 1.44	data + 9.05
data	0	1	DATA- $\overline{\text{SYNC}}$	data + 1.44	data + 1.44
$00	1	1	BLACK	1.44	9.05
$00	0	1	BLACK- $\overline{\text{SYNC}}$	1.44	1.44
$XX	1	0	$\overline{\text{BLANK}}$	0	7.62
$XX	0	0	$\overline{\text{SYNC}}$	0	0

Note: 75 Ω doubly terminated load, SETUP = logic high. V_{REF} = 1.235 V, RSET = 147 Ω.

Functional Description (continued)

DAC Gain (continued)

NO $\overline{\text{SYNC}}$		$\overline{\text{SYNC}}$	
mA	V	mA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000

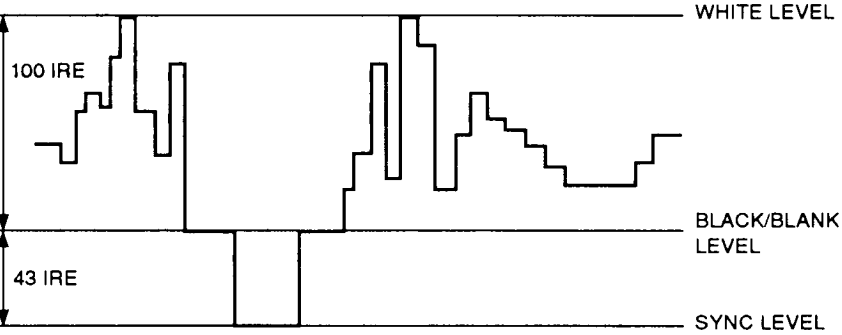


Figure 7. RS-343A Composite Video Output Waveforms

Table 12. RS-343A Video Output Truth Table (no blank offset current)

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	IOUT (mA) $\overline{\text{SYNC}}$ Disabled	IOUT (mA) $\overline{\text{SYNC}}$ Enabled
$FF	1	1	WHITE	17.62	25.24
data	1	1	DATA	data	data + 7.62
data	0	1	DATA- $\overline{\text{SYNC}}$	data	data
$00	1	1	BLACK	0	7.62
$00	0	1	BLACK- $\overline{\text{SYNC}}$	0	0
$XX	1	0	$\overline{\text{BLANK}}$	0	7.62
$XX	0	0	$\overline{\text{SYNC}}$	0	0

Note: 75 Ω doubly terminated load, SETUP = logic low. V_{REF} = 1.235 V, RSET = 147 Ω.

Functional Description (continued)

DAC Gain (continued)

NO $\overline{\text{SYNC}}$		$\overline{\text{SYNC}}$	
mA	V	mA	V
14.25	0.713	20.36	1.018
0.00	0.000	6.11	0.305
0.00	0.000	0.00	0.000

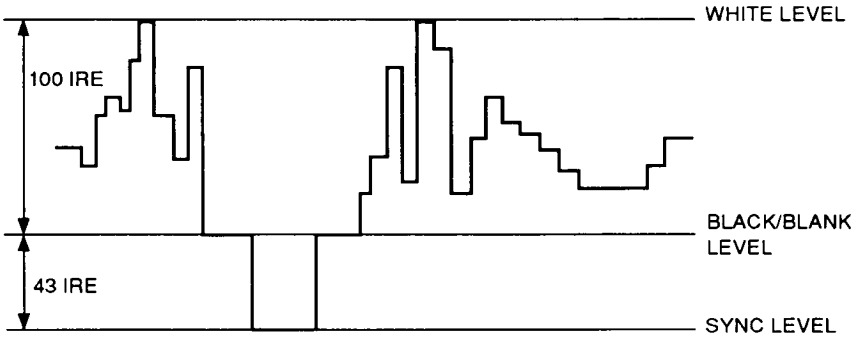


Figure 8. *PS/2* Composite Video Output Waveforms

Table 13. *PS/2* Video Output Truth Table

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	$\overline{\text{SYNC}}$ Disabled I_{OUT} (mA)	$\overline{\text{SYNC}}$ Enabled I_{OUT} (mA)
$FF	1	1	WHITE	14.25	20.36
data	1	1	DATA	data	data + 6.11
data	0	1	DATA- $\overline{\text{SYNC}}$	data	data
$00	1	1	BLACK	0	6.11
$00	0	1	BLACK- $\overline{\text{SYNC}}$	0	0
$XX	1	0	$\overline{\text{BLANK}}$	0	6.11
$XX	0	0	$\overline{\text{SYNC}}$	0	0

Note: 50 Ω load, SETUP = logic low. V_{REF} = 1.235 V, RSET = 182 Ω.

Application Information

Board Layout

Careful configuration and placement of supply planes, components, and signal traces ensure a low-noise board. This also helps ensure proper functionality and low signal emissions in restricted frequency bands as mandated by regulatory agencies.

A four-layer PC board with separate power and ground planes will likely result in a board with quieter signals and supplies as well as less spectral content in emitted frequency bands. The board should have signal layers 1 and 4 (outside layers) and supply layers 2 and 3 (inside layers). Use a solid ground plane for frequencies below 80 MHz. A solid or a split ground plane can be used for frequencies above 80 MHz.

The ATT20C491 should be placed close to the video output connector and between the video output connector and the edge card connector. This will keep the high-speed DAC output traces short and minimize the amount of circuitry between the RAMDAC and the supply pins on the edge card connector.

Power Distribution

Separate the power plane into digital and analog areas. Place all digital components over the digital plane and all analog components over the analog plane. The analog components include the RAMDAC, reference circuitry, comparators, all mixed signal chips (such as a clock synthesizer), and any passive support components for analog circuits.

The analog and digital power plane should be connected with at least one ferrite bead across the separation, as illustrated in Figures 9 and 10. This bead provides resistance to high-frequency currents. Select a ferrite bead with an impedance curve suitable for your design. The ferrite should have a resistance at a higher frequency than the maximum signal frequency on the board, but lower than the second harmonic (2x) of that frequency. The following beads provide resistances of approximately 75 Ω at 100 MHz: Ferroxcube VK20019-4B, Fair-Rite 2743001111, or Philips 431202036690.

Decoupling Capacitors

All decoupling capacitors should be located within 0.25 in. of the device to be decoupled. Chip capacitors are recommended, but radial and axial leads will work. Keep lead lengths as short as possible to reduce inductance and EMI. For leaded capacitors, use devices with a self-resonance above the pixel clock frequency.

For the ATT20C491, decouple Vcc pins 21 and 22 to ground with a 0.01 µF capacitor. Decouple Vcc pin 4 to ground with a 0.01 µF capacitor. For higher-frequency pixel clocks (>80 MHz), use a 0.01 µF capacitor in parallel with the 0.1 µF capacitor to shunt the higher-frequency noise to ground. Power supply noise should be less than 200 mV for a good design. About 10% of any noise below 1 MHz will be coupled onto the DAC outputs. As illustrated in Figures 7 and 8, the COMP pin should also be decoupled with a 0.1 µF capacitor. For designs showing ghosting or smearing, add a parallel COMP capacitance of 2.2 µF.

Digital Signals

The digital inputs should not travel over the analog power plane if possible. The RAMDAC should be located over the analog plane close to the digital/analog supply separation. The RAMDAC may also be placed over the supply separation so the digital pixel inputs are over the digital supply plane. The digital inputs, especially the P[7:0] high-speed inputs, should be isolated from the analog outputs. Placing the digital inputs over the digital supply reduces coupling into the analog supply plane. High-speed signals (both analog and digital) should not be routed under the RAMDAC.

Avoid high slew rate edges since they can contribute to undershoot, overshoot, ringing, EMI, and noise feedthrough. Wherever possible, use slower edge rate (2 ns—4 ns) logic such as 74S or 74ALS devices. If this is not possible, edges can be slowed down by using series termination (75 Ω to 150 Ω). Edge noise will result if the digital signal propagates from an impedance mismatch while the signal rises. The reflection noise is particularly troublesome in the TTL threshold region. For a 2 ns edge, the trace length must be less than 4 in.

Application Information (continued)

Digital Signals (continued)

The clock signal trace should be as short as possible and should not run parallel to any high-speed signals. To ensure a quality clock signal without high-frequency noise components, decouple the supply pins on the clock driver. If necessary, transmission line techniques should be used on the clock by providing controlled impedance striplines and parallel termination.

Analog Signals

The load resistor should be as close as possible to the DAC outputs. The resistor should equal the destination termination which is usually a 75 Ω monitor. Unused analog outputs should be connected to ground. The DAC output traces should be as short as possible to minimize any impedance mismatch in the trace or video connector.

Series ferrite beads can be added to the analog video signal to reduce high-frequency signals coupled onto the DAC outputs or reflected from the monitor.

To reduce the interaction of the analog video return current with board components, a separate video ground return trace can be added to the ground plane or signal layer. This trace connects directly to the point that ground enters the card.

DAC Outputs

The ATT20C491/492 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching ac coupled monitors.

The diode protection circuit shown in Figures 9 and 10 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes.

Application Information (continued)

DAC Outputs (continued)

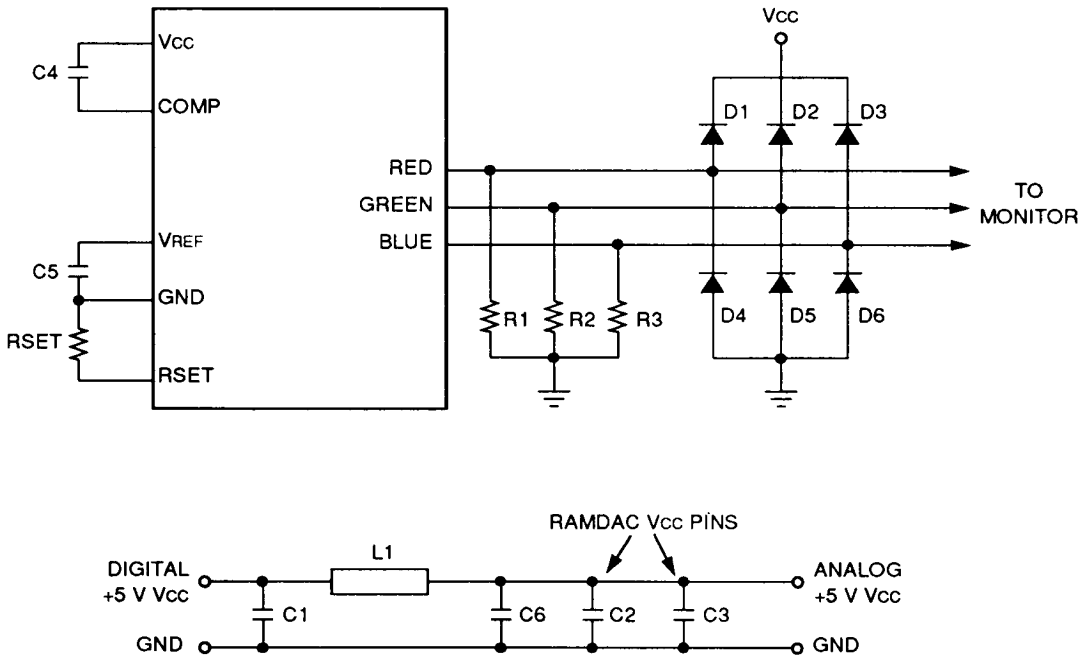


Figure 9. Typical Connection Diagram Using the Internal Voltage Reference

Table 14. Internal Voltage Reference Parts List

Location	Description	Vendor Part Number
C1—C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	Ferrite bead	Fair-Rite 2743001111
R1—R3	75 Ω, 1% metal film resistor	Dale CMF-55C
RSET	147 Ω, 1% metal film resistor	Dale CMF-55C
D1—D6	Fast-switching diodes	National 1N4148/49

Note: The above vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the ATT20C491.

Application Information (continued)

DAC Outputs (continued)

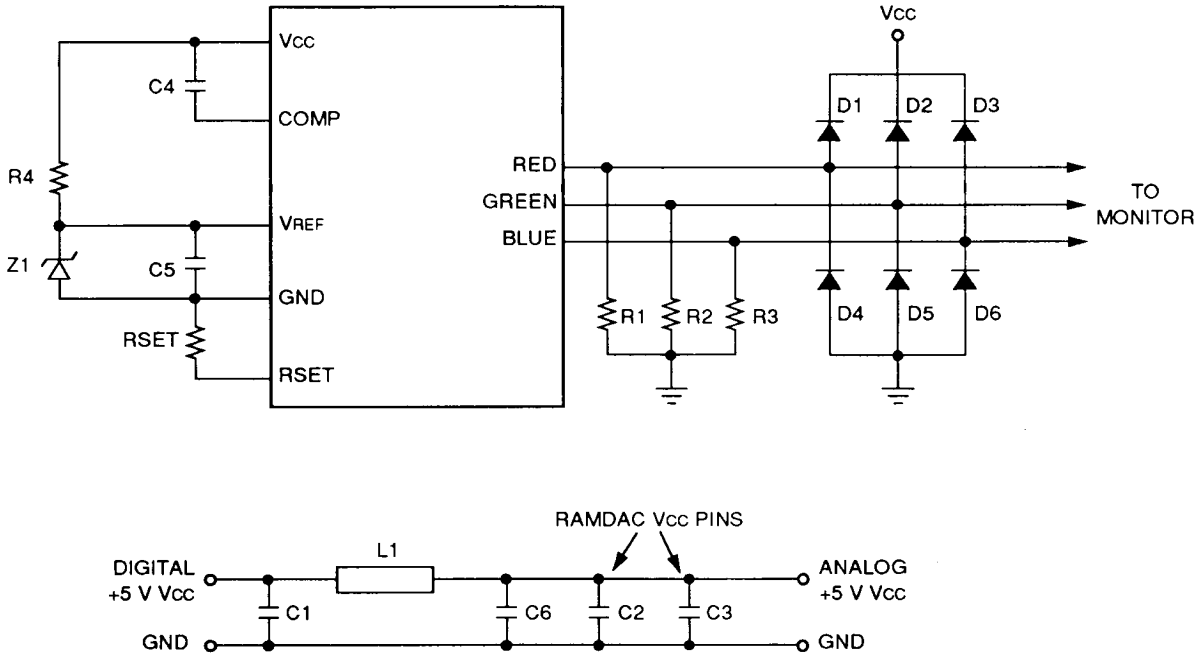


Figure 10. Typical Connection Diagram Using an External Voltage Reference

Table 15. External Voltage Reference Parts List

Location	Description	Vendor Part Number
C1—C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	Ferrite bead	Fair-Rite 2743001111
R1—R3	75 Ω, 1% metal film resistor	Dale CMF-55C
R4	1 kΩ, 5% resistor	—
RSET	147 Ω, 1% metal film resistor	Dale CMF-55C
Z1	1.2 voltage reference	National Semiconductor LM385BZ-1.2
D1—D6	Fast-switching diodes	National 1N4148/49

Note: The above vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the ATT20C491.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
Vcc (measured to GND)	—	—	—	7.0	V
Voltage on Any Digital Pin	—	GND – 0.5	—	Vcc + 0.5	V
Analog Output Short Circuit: Duration to Any Power Supply or Common	ISC	—	indefinite	—	—
Ambient Operating Temperature	T_A	–55	—	125	°C
Storage Temperature	T_{stg}	–65	—	150	°C
Junction Temperature	T_J	—	—	150	°C
Vapor Phase Soldering (60 s)	T_{VSOL}	—	—	220	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply (MHz)	V_{CC}	4.75	5.00	5.25	V
Ambient Operating Temperature	T_A	0	—	70	°C
Output Load	R_L	—	37.5	—	Ω
Reference Voltage	V_{REF}	1.2	1.235	1.27	V

Electrical Characteristics

Table 16. dc Characteristics

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = 7.5 IRE, 8/$\overline{6}$ pin = logic 1. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Parameter	Symbol	Min	Typ	Max	Unit
Resolution (each DAC):	—	6	6	8	bits
Accuracy (each DAC):					
Integral Linearity Error	IL	—	—	±1 (±1/4)	LSB
Differential Linearity Error	DL	—	—	±1 (±1/4)	LSB
Gain Error	—	—	—	±5	%
Monotonicity	—	—	guaranteed	—	Scale
Coding	—	—	—	—	Binary
Digital Inputs:					
Input Voltage:					
Low	V_{IL}	GND – 0.5	—	0.8	V
High	V_{IH}	2.0	—	V_{CC} + 0.5	V
Input Current:					
Low (V_{IN} = 0.4 V)	I_{IL}	—	—	–1	µA
High (V_{IN} = 2.4 V)	I_{IH}	—	—	1	µA
Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	C_{IN}	—	—	7	pF
Digital Outputs:					
Output Voltage:					
Low (I_{OL} = 3.2 mA)	V_{OL}	—	—	0.4	V
High (I_{OH} = –400 µA)	V_{OH}	2.4	—	—	V
3-State Current	Ioz	—	—	50	µA
Capacitance	C_{DOUT}	—	—	7	pF
Analog Outputs:					
Gray Scale Current Range	Igray	—	—	20	mA
Output Current:					
White Level Relative to Black	Iwb	16.74	17.62	18.50	mA
Black Level Relative to Blank:	Ibb				
Setup = Logic High		0.95	1.44	1.90	mA
Setup = Logic Low		0	5	50	µA
Blank Level:	Iblank				
Sync Enabled		6.29	7.62	8.96	mA
Sync Disabled		0	5	50	µA
LSB Size:	Ilsb				
6-bit DACs		—	279.68	—	µA
8-bit DACs		—	61.1	—	µA
DAC to DAC Matching	—	—	2	5	%
Output Compliance	V_{OC}	–0.5	—	1.5	V
Output Impedance	RA_{OUT}	—	10	—	kΩ
Output Capacitance (f = 1 MHz, I_{OUT} = 0 mA)	CA_{OUT}	—	—	30	pF
Internal Reference Output (±3%)	V_{REF}	1.2	1.235	1.27	V
Power Supply Rejection Ratio: (COMP = 0.1 F, f = 1 kHz)	PSRR —	— —	— —	0.5 –6	%/% ΔV_{CC} dB

Electrical Characteristics (continued)

Table 17. ac Characteristics

Test conditions generate RS-343 video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = 7.5 IRE, $\overline{8/6}$ = logic 1. The parameters are applicable over the full voltage and temperature range as shown in the Recommended Operating Conditions table.

		100 MHz Devices			80 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Clock Rate	fmax	—	—	100	—	—	80	MHz
RS[2:0] Setup Time	1	10	—	—	10	—	—	ns
RS[2:0] Hold Time	2	10	—	—	10	—	—	ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5	—	—	5	—	—	ns
$\overline{RD}$ Asserted to Data Valid	4	—	—	30	—	—	40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5	—	—	20	—	—	20	ns
Read Data Hold Time	6	5	—	—	5	—	—	ns
Write Data Setup Time	7	10	—	—	10	—	—	ns
Write Data Hold Time	8	10	—	—	10	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50	—	—	50	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10, 11	6	—	—	6	—	—	PCLK
Pixel and Control Setup Time	12	2	—	—	3	—	—	ns
Pixel and Control Hold Time	13	2	—	—	3	—	—	ns
Clock Cycle Time (PCLK)	14	10	—	—	12.5	—	—	ns
Clock Pulse Width High Time	15	3	—	—	4	—	—	ns
Clock Pulse Width Low Time	16	3	—	—	4	—	—	ns
Analog Output Delay	17	—	—	30	—	—	30	ns
Analog Output Rise/Fall Time	—	—	2	—	—	2	—	ns
Analog Output Settling Time*	—	—	10	—	—	13	—	ns
Clock and Data Feedthrough*	—	—	–30	—	—	–30	—	dB
Glitch Impulse*	—	—	75	—	—	75	—	pV-s
DAC to DAC Crosstalk	—	—	–23	—	—	–23	—	dB
Analog Output Skew	18	—	—	2	—	—	2	ns
$\overline{SENSE}$ Output Delay	—	—	1	—	—	1	—	µs
Pipeline Delay	—	4	—	8	4	—	8	Clocks
V_{CC} Supply Current† Normal Operation	I_{CC}	—	140	200	—	135	190	mA
Sleep Mode‡	ISLP							
PCLK = 1 MHz	—	—	3	5	—	3	5	mA
PCLK = 35 MHz	—	—	5	10	—	5	10	mA

* Clock and data feedthrough are functions of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74 HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough. –3 dB test bandwidth = 2 x clock rate.

† At fmax, I_{CC} (typ) at V_{CC} = 5.0 V I_{CC} (max) at V_{CC} (max).

‡ External current or voltage reference automatically disabled during sleep mode. Test conditions: 25 °C to 70 °C. Pixel and data ports at 0.4 V.

Electrical Characteristics (continued)

Table 17. ac Characteristics (continued)

Test conditions generate RS-343 video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, $\overline{8/6}$ = logic 1. The parameters are applicable over the full voltage and temperature range as shown in the Recommended Operating Conditions table.

		66 MHz Devices			55 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Clock Rate	fmax	—	—	66	—	—	50	MHz
RS[2:0] Setup Time	1	10	—	—	10	—	—	ns
RS[2:0] Hold Time	2	10	—	—	10	—	—	ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5	—		5	—	—	ns
$\overline{RD}$ Asserted to Data Valid	4	—	—	40	—	—	40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5	—	—	20	—	—	20	ns
Read Data Hold Time	6	5	—	—	5	—	—	ns
Write Data Setup Time	7	10	—	—	10	—	—	ns
Write Data Hold Time	8	10	—	—	10	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50	—	—	50	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10, 11	6	—	—	6	—	—	PCLK
Pixel and Control Setup Time	12	3	—	—	3	—	—	ns
Pixel and Control Hold Time	13	3	—	—	3	—	—	ns
Clock Cycle Time (PCLK)	14	15.15	—	—	18.2	—	—	ns
Clock Pulse Width High Time	15	5	—	—	7.3	—	—	ns
Clock Pulse Width Low Time	16	5	—	—	7.3	—	—	ns
Analog Output Delay	17	—	—	30	—	—	30	ns
Analog Output Rise/Fall Time	—	—	2	—	—	3	—	ns
Analog Output Settling Time*	—	—	13	—	—	20	—	ns
Clock and Data Feedthrough*	—	—	-30	—	—	-30	—	dB
Glitch Impulse*	—	—	75	—	—	75	—	pV-s
DAC to DAC Crosstalk	—	—	-23	—	—	-23	—	dB
Analog Output Skew	18	—	—	2	—	—	2	ns
$\overline{SENSE}$ Output Delay	—	—	1	—	—	1	—	µs
Pipeline Delay	—	4	—	8	4	—	8	Clocks
VCC Supply Current† Normal Operation	ICC	—	120	180	—	115	175	mA
Sleep Mode‡	ISLP							
PCLK = 1 MHz	—	—	3	5	—	3	5	mA
PCLK = 35 MHz	—	—	5	10	—	5	10	mA

* Clock and data feedthrough are functions of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74 HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough. –3 dB test bandwidth = 2 x clock rate.

† At fmax, ICC (typ) at VCC = 5.0 V ICC (max) at VCC (max).

‡ External current or voltage reference automatically disabled during sleep mode. Test conditions: 25 °C to 70 °C. Pixel and data ports at 0.4 V.

Timing Characteristics

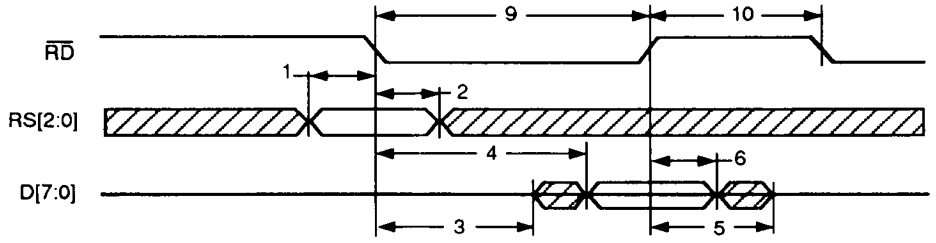


Figure 11. Basic Read-Cycle Timing Diagram

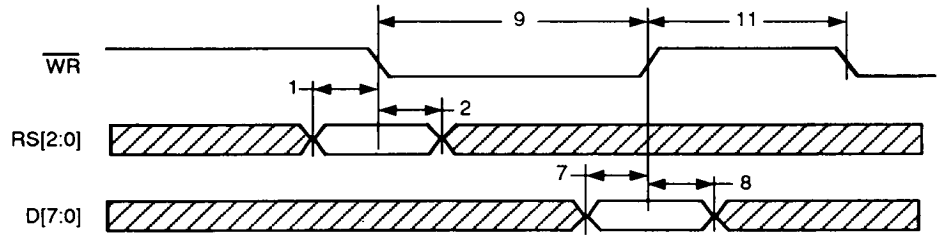


Figure 12. Basic Write-Cycle Timing Diagram

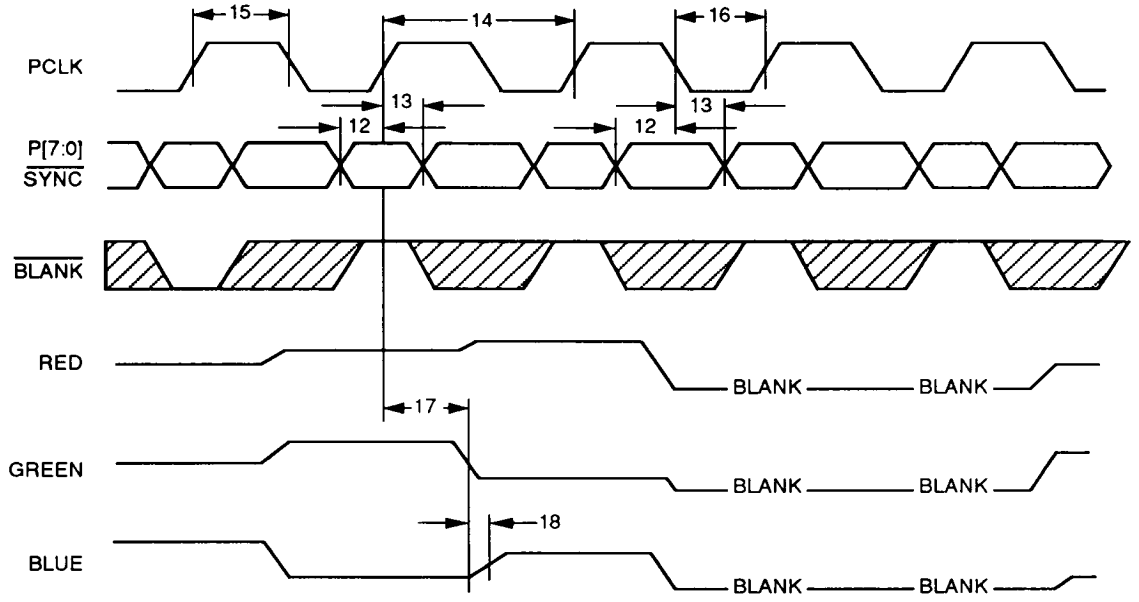


Figure 13. Pixel and Video Control Timing

Timing Characteristics (continued)

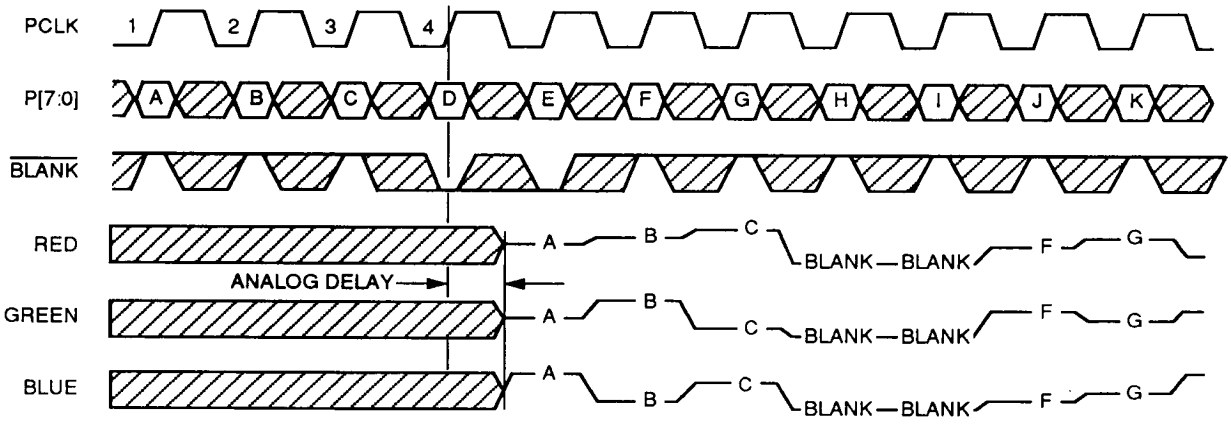


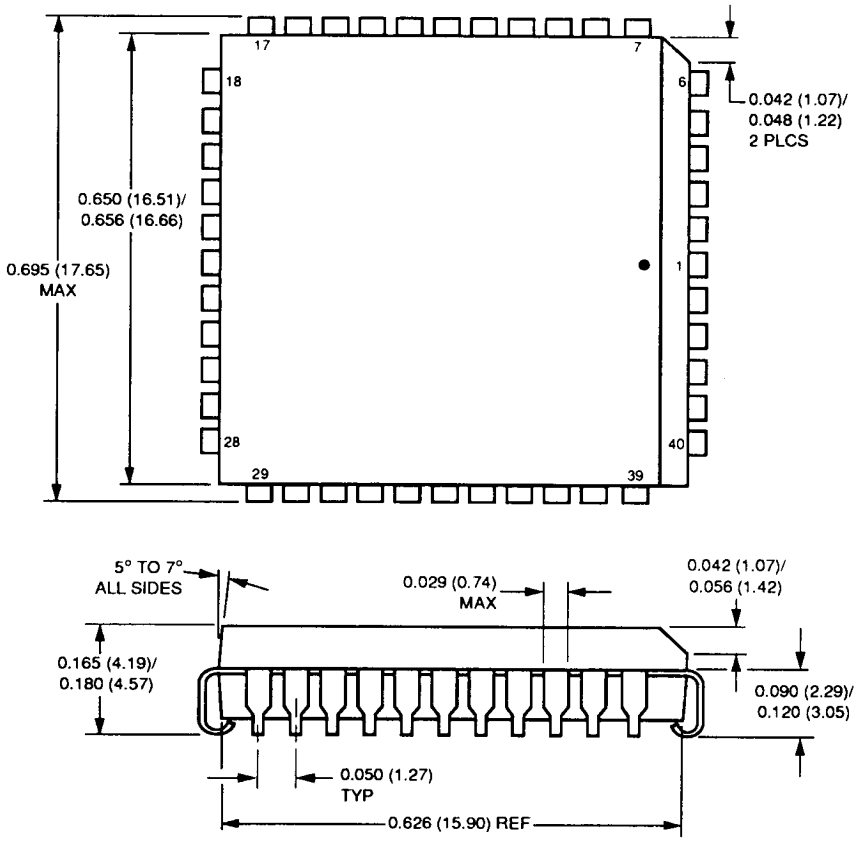
Figure 14. System Timing Diagram: Pixel Pipeline

Outline Diagram

44-Pin PLCC Package

Top View.

Dimensions are in inches and (millimeters).



Ordering Information

Device*	Speed	Package Type
ATT20C491-XXM44	100/80/66 MHz	44-Pin PLCC
ATT20C492-XXM44	100/80/66/55 MHz	44-Pin PLCC

* XX refers to speed grade:
10 = 100 MHz
80 = 80 MHz
66 = 66 MHz
55 = 55 MHz

For additional information, contact your AT&T Account Manager or the following:
U.S.A.: AT&T Microelectronics, Dept. AL-520404200, 555 Union Boulevard, Allentown, PA 18103
1-800-372-2447, FAX 215-778-4106 (In CANADA: **1-800-553-2448,** FAX 215-778-4106)
EUROPE: AT&T Microelectronics, AT&T Deutschland GmbH, Bahnhofstr. 27A, D-8043 Unterfoehring, Germany
Tel. (49) 89 95086-0, FAX (49) 89 95086-331
ASIA PACIFIC: AT&T Microelectronics Asia/Pacific, 14 Science Park Drive, #03-02A/04 The Maxwell, Singapore 0511
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